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HIGH Q VARACTOR DIODES

FINAL TECHNICAL SUMMARY REPORT

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by

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I. ABSTRACT

Low pump power varactor diodes have been fabricated using epitaxial GaAs. Frequency cut-offs as high as 785 KMC have been obtained at breakdown. A detailed analysis of the parameters influencing point-contact GaAs varactors is given.

The results of a basic program to determine the feasibility of employing high energy gap semiconductors in varactor diodes are presented. The voltage breakdown and capacitance of abrupt large area P^{++} on N GaAs diodes have been determined as a function of resistivity. Square law behavior is observed up to breakdown. The electrical properties of P^{++} on N large area GaP diodes are also given.

The HCl carrier gas technique and "The Travelling Solvent Method of Crystal Growth" have been employed in the epitaxial growth of GaAs and GaP on GaAs, GaP, and Ge substrates. The properties of GaAs-GaP, GaP-Ge, and GaAs-Ge heterojunctions are presented.

Low pump power varactor diodes have been fabricated using epitaxial GaP as the active semiconductor (GaP deposited on 0.0007 Ω-cm GaAs). Frequency cut-offs of 187 KMC at -2V have been obtained using this N on N^{++} configuration.

II. POINT CONTACT VARACTORS

A. VARACTOR PROPERTIES

The two basic properties of a varactor diode which are important for parametric action are junction capacity, C(V); and resistance, R_s. These two quantities are related by the expression:

$$Q(V) = \frac{1}{\omega C(V) R_s} \qquad (1)$$

where ω is the radial frequency and Q is the quality factor.

In general, the capacitance of a P-N junction as a function of voltage, V, is given by the familiar equation

$$C = C_o \left[1 - V/\phi\right]^{-1/n} \qquad (2)$$

where C_o is the capacity with zero bias, and ϕ is the potential at which the capacity becomes infinite. n = 2 for an abrupt junction or n = 3 for a graded junction. Point contact GaAs junctions are abrupt. The resistance is made up of not only the spreading resistance, but any other loss associated with the varactor.

Sometimes a cut-off frequency, f_c, is used to indicate the quality of the varactor. This is the calculated value of the frequency at which Q = 1 or,

$$f_c = \frac{1}{2\pi C(V) R_s} \qquad (3)$$

As f_c depends on the voltage, when varactors are compared it is important that this be done at the same value of bias.

In addition to the capacity and resistance, subsidiary parameters, like package inductance and package capacitance are important in physically realizable devices, and should be small. In principle, the parastic impedance of the package may be tuned out by other elements in the parametric device, but this reduces the bandwidth.

The capacity of the junction per unit area can be shown to be in the form of:

$$C = \left[\frac{\epsilon}{\mu \rho (V + \phi)}\right]^{1/n} A \qquad (4)$$

where ϵ is the dielectric constant, ρ is the resistivity, μ is the mobility, ϕ is the built-in potential, and A is the junction area. Therefore, C_o in equation (1) is

$$C_o = \left[\frac{\epsilon}{\mu \rho \phi}\right]^{1/n} A \qquad (5)$$

Small values of the capacity occur for large mobility, large resistivity and large ϕ. In general, the value of C_o should be low enough so that the capacitive reactance is not too small. For example, for a reactance of 50 ohms at 10 KMC, $C_o = 0.31$ pf.

From Eq. (1) we see that for a high Q device the capacity and resistance should be small. The resistance is determined by the spreading resistance, which for a spherical contact of radius r_o and resistivity ρ is $R_s = \rho / 2\pi r_o$.

This requires that the resistivity should be low, but it is necessary that ρ be large enough so as to give a reasonable value of the breakdown voltage, V_B. Therefore, some compromise value of ρ must be chosen. In order to achieve this proper balance of voltage breakdown, series resistance, and capacitance using homogeneous GaAs, the chip would have to be extremely thin (about 5-10 microns). The earliest attempts here to avoid the difficulties inherent in such thin chips were based on the use of out-diffusion of N-type impurity from the surface of low resistivity GaAs. This yielded a structure having a relatively high resistivity surface. Although excellent varactors having high Q and high f_{co} were made using this technique, the yield of such devices was unsatisfactorily low. The logical extension of this approach is to use an epitaxial N-on-N^+ material.

The high resistance of the epitaxial layer gives a high breakdown and the low resistivity substrate keeps R_s small. An approximate solution to the problem for a contact of radius r_o, epitaxial layer of resistivity ρ_e and thickness δ, on a substrate of resistivity ρ_s, gives

$$R_s = \frac{\rho_e}{2\pi(r_o + \delta)}\left[\frac{\delta}{r_o} + \frac{\rho_s}{\rho_e}\right] \qquad (6)$$

This means that in order to substantially decrease the spreading resistance without effecting the breakdown, $\rho_s << \rho_e$ and $\delta << r_o$.

In theory, it is possible to make epitaxial wafers having a precalculated optimum combination of N-on-N^+ properties. In practice, however, the only present source of epitaxial GaAs is the Monsanto Chemical Corporation, and they have so far been unable to supply wafers made to order with accurately specified properties. Instead, we have made sample varactors from a fairly wide range of wafers differing in substrate dopant, doping level, and orientation, and in eptiaxial layer resistivity, mobility, and thickness. On the basis of these results, which are summarized in Table I, we conclude the following:

a. The substrate should be of (111) orientation, with the epitaxial layer on the B-face;

b. The substrate should have the minimum possible resisitivity;

c. The substrate dopant may be either Se or Te;

d. The epitaxial layer should be between 3 and 6 microns thick;

e. The mobility of carriers in the epitaxial layer should be as high as possible;

f. The resisitivity of the epitaxial layer should be about 0.06 ohm-cm.

TABLE I

Epitaxial GaAs Sample Data

Lot No.	n per cm^3	μ cm^2 volt-sec.	p ohm-cm	t microns	Layer type	Dopant	Orient.	Break-down voltage	f_{c-2V} (kmc)	C_{jo} (pf.)
81, 81A	6×10^{18}	1540	6.3×10^{-4}	(20 mils)	substrate	Te	111-B	8-12	150	.25
	2×10^{16}	5000	.058	6.5	epitaxial					
82	$2.3 - 6.4 \times 10^{18}$	1540-3090	6.8×10^{-4}	(20 mils)	substrate	Te	111-B	7-10	80	.15
	3.9×10^{16}	5200	.031	6.8-7.1	epitaxial					
83	4.36×10^{18}	2310	7.5×10^{-4}	-	substrate	Te	111-B	7-9	115	.23
	5.9×10^{15}	5450	0.19	4.5	epitaxial					
84	-	-	11×10^{-4}	-	substrate	Te	100	8-11	60	.23
	-	-	.05	6.8	epitaxial					
85	-	-	7×10^{-4}	-	substrate	Se	111-B	6-8	170*	.28
	-	-	.046	1.3	epitaxial					

*Incomplete sampling; 70% of units shorted through due to thin epitaxial layer.

1. Capacity Measurements

In general, the total capacity of an abrupt junction varactor diode is the following function of voltage, V:

$$C_T(V) = C_p + C_{jo}(1 - V/\phi)^{-1/2} \qquad (7)$$

where $C_T(V)$ is the total capacity, C_p the capacity of the package, C_{jo} the junction capacity at zero bias, and ϕ a constant depending on the material. In order to verify this behavior, a detailed series of measurements was made of the capacity at 1 mc as a function of voltage on several diodes. In the analysis of the data a value of ϕ was assumed and $C_T(V)$ was plotted versus $(1 - V/\phi)^{-1/2}$ (Fig. 1). As $(1 - V/\phi)^{-1/2} \to 0$, then $C_T(V) \to C_p$, so C_p is just the ordinate intercept. Using this value of C_p, $\left[\frac{1}{C_T(V) - C_p}\right]^2$ was plotted as a function of V. (Fig. 2). Since

$$\left[\frac{1}{C_T(V) - C_p}\right]^2 = \frac{1}{C_{jo}^2} = (1 - V/\phi), \qquad (8)$$

ϕ is the x intercept. By using the corrected value of ϕ, C_p can be redetermined, etc., until self-consistant values of C_p and ϕ are found. Usually only one or two tries are necessary to give a very good fit.

On all the point contact varactors on which this series of measurements have been made, the data can be fit very well by assuming that the exponent of the voltage dependence is 1/2, but ϕ varies somewhat from material to material, having a range from 1.0 to approximately 1.3 volts for GaAs.

In principle, it should be possible to determine not only the value of C_p, C_{jo}, and ϕ, but also the value of the exponent. Generally, a value of n is assumed (Eq. 2) and the other parameters are determined. If these parameters give a good fit to the data, it is then assumed that the choice of n was correct. For a large area junction of P-type GaAs deposited epitaxially on N-type Ge, the value of n was varied to see if a better fit

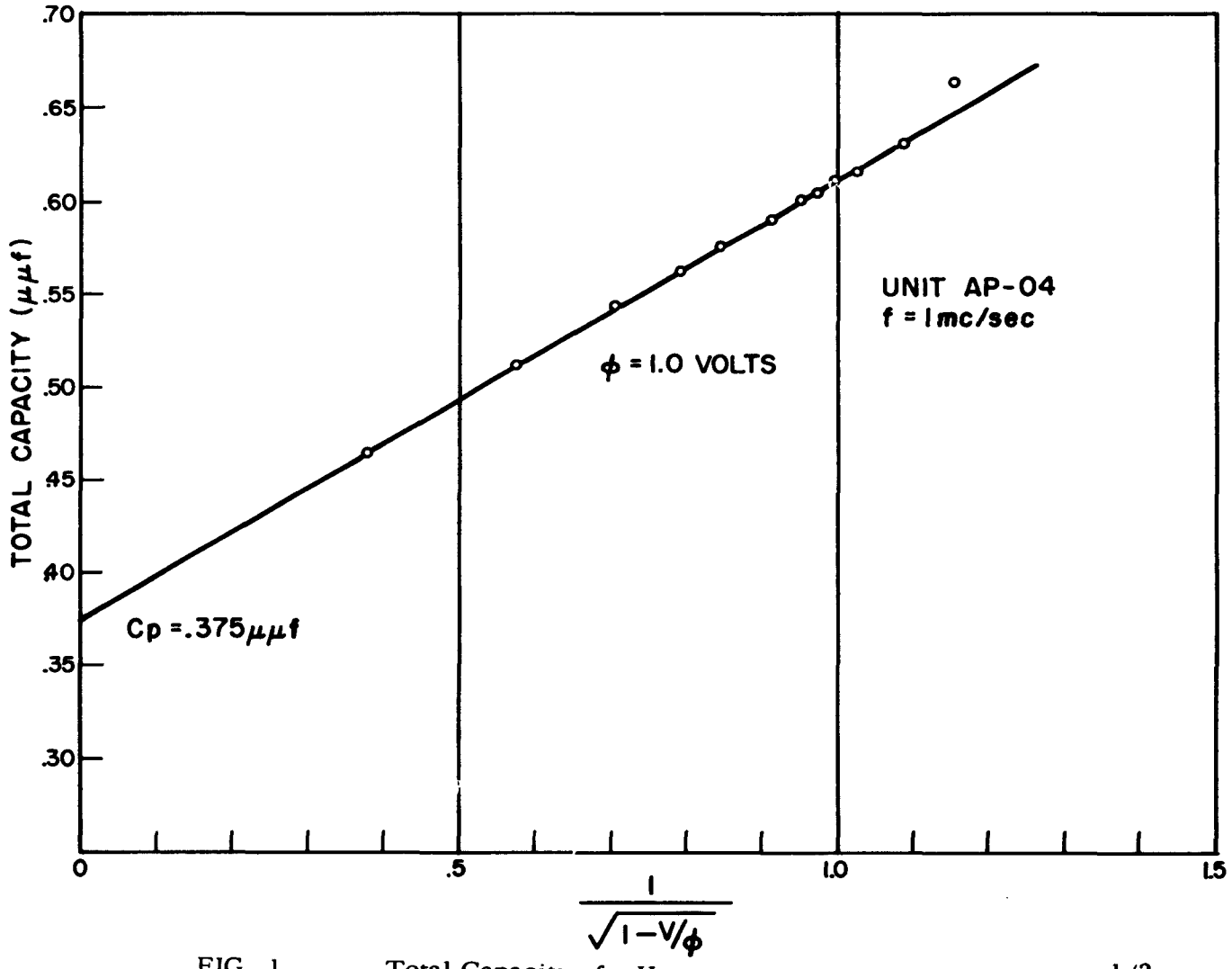

FIG. 1 Total Capacity of a Varactor as a Function of $(1 - V/\phi)^{-1/2}$

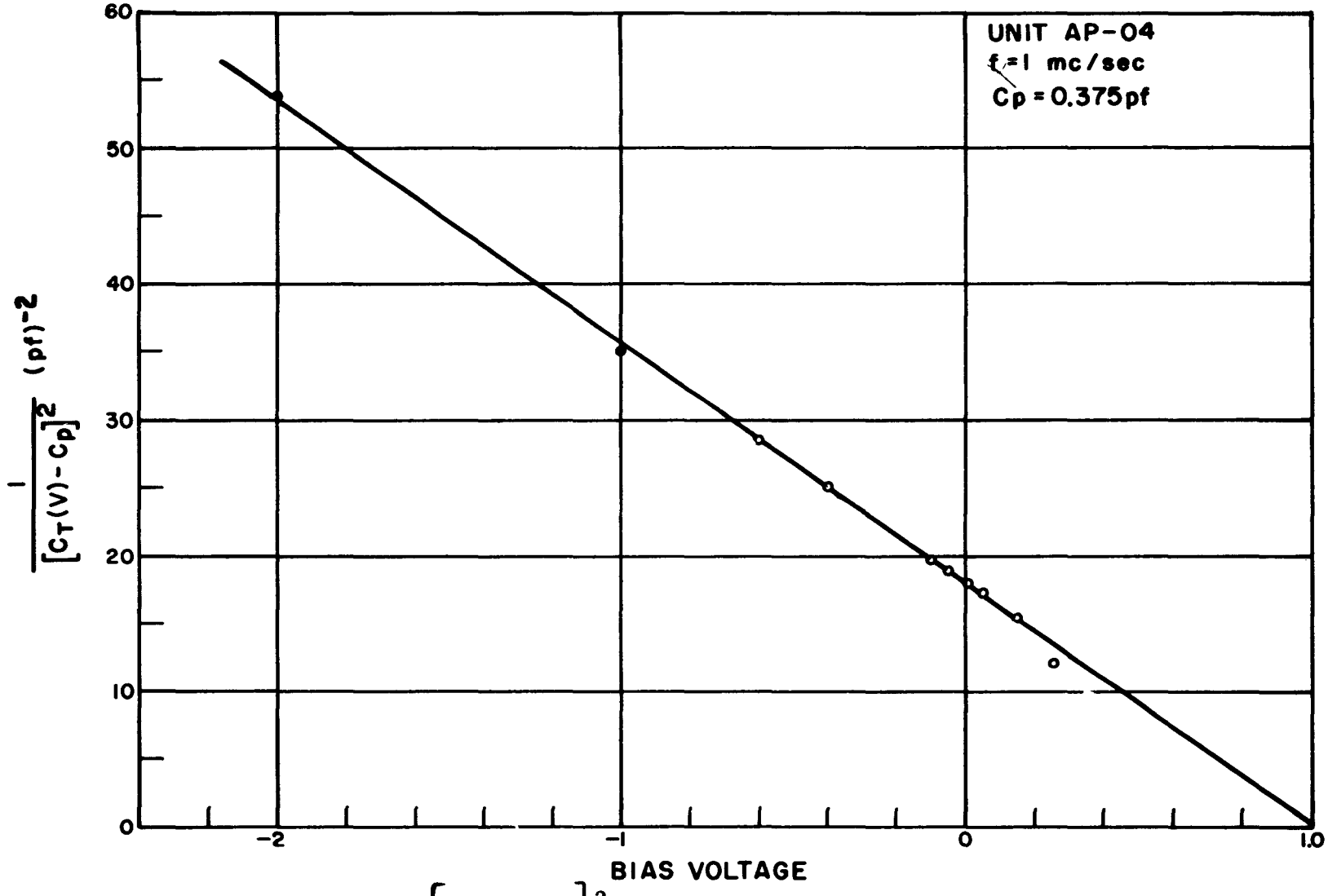

FIG. 2 $\left[\frac{1}{C_T(V) - C_p}\right]^2$ vs. the Bias Voltage for Varactor Diode

could be obtained. This was done by assuming various values for n and making a least square fit to determine ϕ and C_o. Table II shows the values of ϕ and C_o as obtained for various values of n along with the rms variation between the calculated and measured values of $1/C^n$. As can be seen, the best fit is for an exponent of .434. C_o shows little change, but ϕ depends critically on the value of n which was chosen.

Measurements made on the capacity of P-N junctions in GaAs give values of ϕ around 1.0 volts; although, in some samples ϕ approximately equal to 1.3 is found. The capacity of a large area junction was measured at 23°C and -195°C as a function of voltage. As shown in Fig. 3 the curve at -196°C is just displaced by a constant amount of 0.20 V with little or no change in slope, which indicates that only ϕ is changing (Eq. 4).

TABLE II

Least Mean Square Values of ϕ and C_o for Various Values of n

Assumed Value of Exponent n	ϕ	C_o	RMS$(\frac{1}{C^n})$
$1.9 = \frac{1}{0.526}$	1.022	165.6	.0055
$2.0 = \frac{1}{0.500}$	.926	166.0	.0044
$2.2 = \frac{1}{0.454}$	.779	166.1	.0020
$2.3 = \frac{1}{0.434}$	.718	166.1	.0009
$2.4 = \frac{1}{0.416}$	.660	166.2	.0021

Least square fit of ϕ and C_o for various assumed values of n for GaAs-Ge heterojunction:

$$\frac{1}{C^n} = \frac{1}{C^n}\ (1-V/\phi)$$

$$\text{RMS}\left(\Delta\ \frac{1}{C^n}\right) = \frac{1}{M}\sqrt{\sum_{i=1}^{M}\left[\frac{1}{C_i^n}\ \text{measured} - \frac{1}{C_i^n}\ \text{calculated}\right]^2}$$

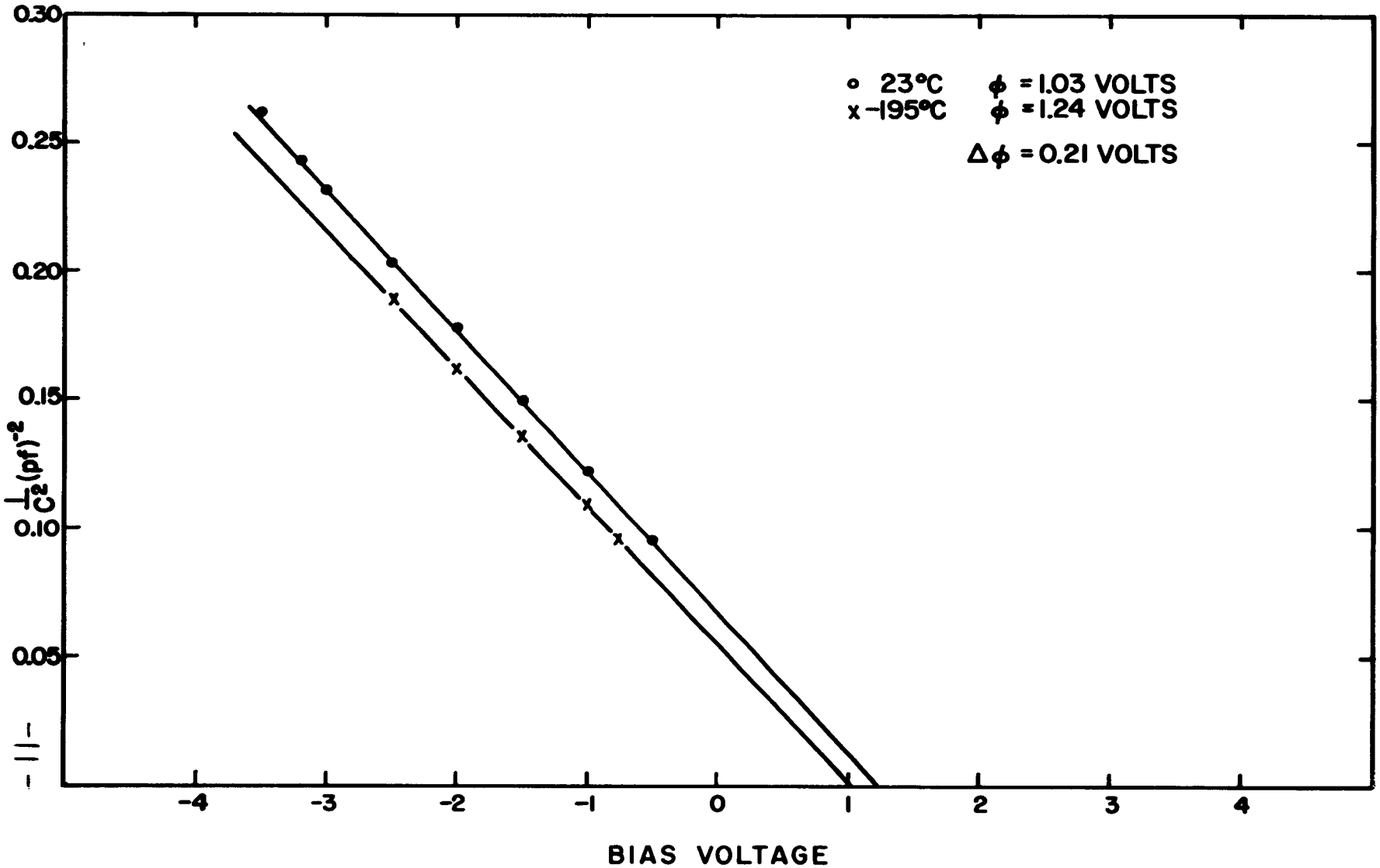

FIG. 3 $1/C^2$ vs. Bias Voltage for a Large Area GaAs P-N Junction

2. Microwave Measurements

In addition to the capacity measurements, microwave measurements of the change in varactor Q, ΔQ, were made. By measuring the VSWR of the varactor as a function of the applied voltage, along with the position of the minimum field in the waveguide, a Smith chart presentation of the data can be made(Fig. 4). After plotting the Smith chart, ΔQ may be determined by rotating the point corresponding to the voltage to the unity resistance circle. ΔQ can also be calculated from the expression:

$$\Delta Q = \frac{VSWR - 1}{\sqrt{VSWR}} \qquad (9)$$

As can be seen in Fig. 4, most points fall on or at least close to the unit circle. Two possible reasons for the points not to fall on the unit circle are:

(1) The resistance of the diode is changing with bias voltage; or

(2) The VSWR is too large to be measured because of holder losses of errors in the slotted line.

For the case of the points corresponding to forward bias, (1) is probably the correct explanation, but explanation (2) is most likely correct for points in the reverse direction.

Another way to present the ΔQ data is to plot ΔQ as a function of the elastance, S. The elastance is just the reciprocal of the capacity of the junction, and may be taken from the 1 mc data. Fig. 5 shows ΔQ as a function of S(V).

$$S(V) = \frac{1}{C_j(V)} = \frac{1}{C_{jo}} (1 - V/\phi)^{1/2} \qquad (10)$$

as $V \rightarrow \phi$, $\Delta Q \rightarrow -Q(V_o)$ where V_o is the bias voltage to which the measurements are referred. This follows, since:

$$\Delta Q(V_1, V_2) = Q(V_1) - Q(V_2) = Q_o \left[(1-V_1/\phi)^{1/2} - (1-V_2/\phi)^{1/2}\right] \qquad (11)$$

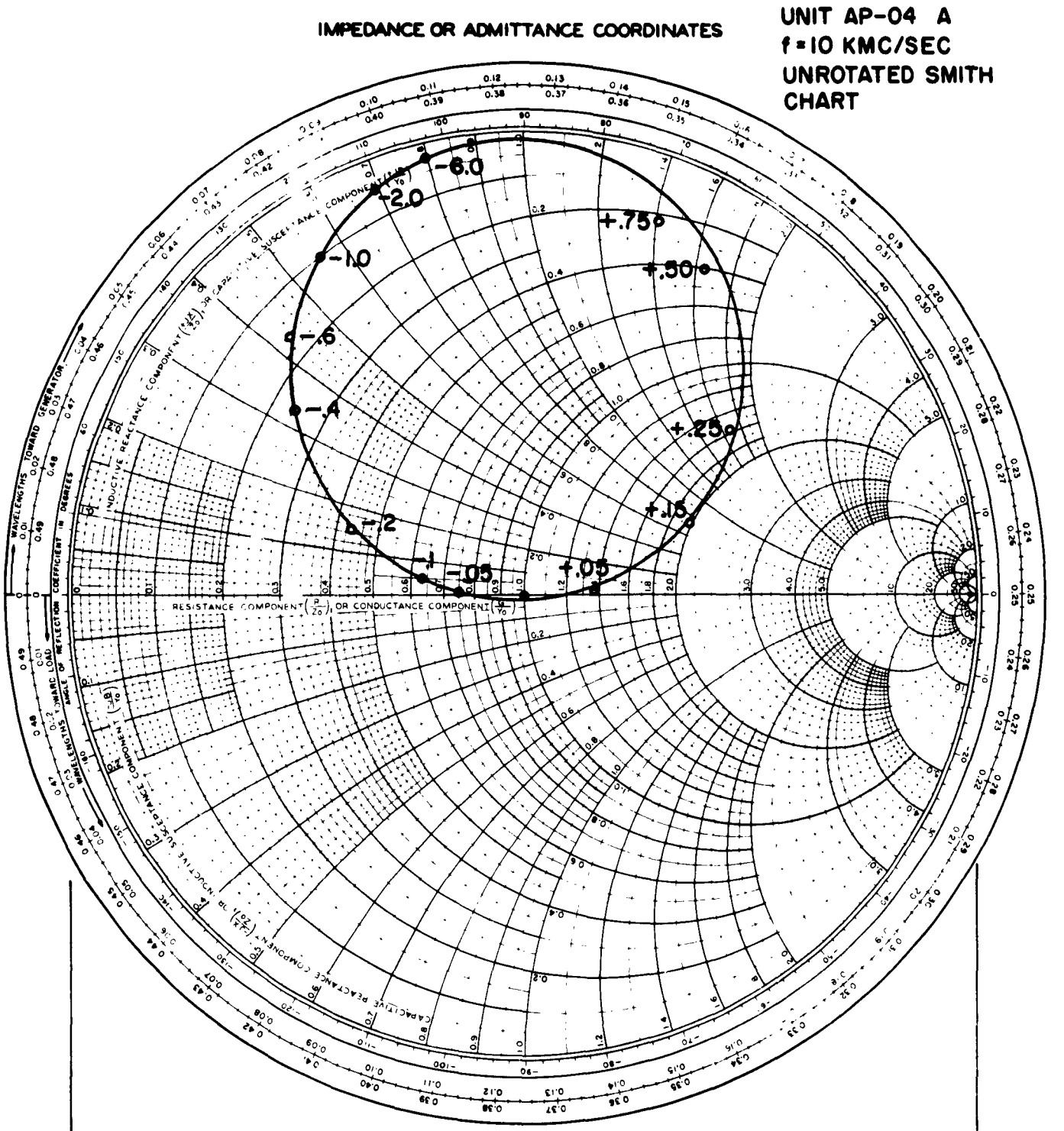

FIG. 4 Unrotated Smith Chart of Varactor Impedance as a Function of Bias

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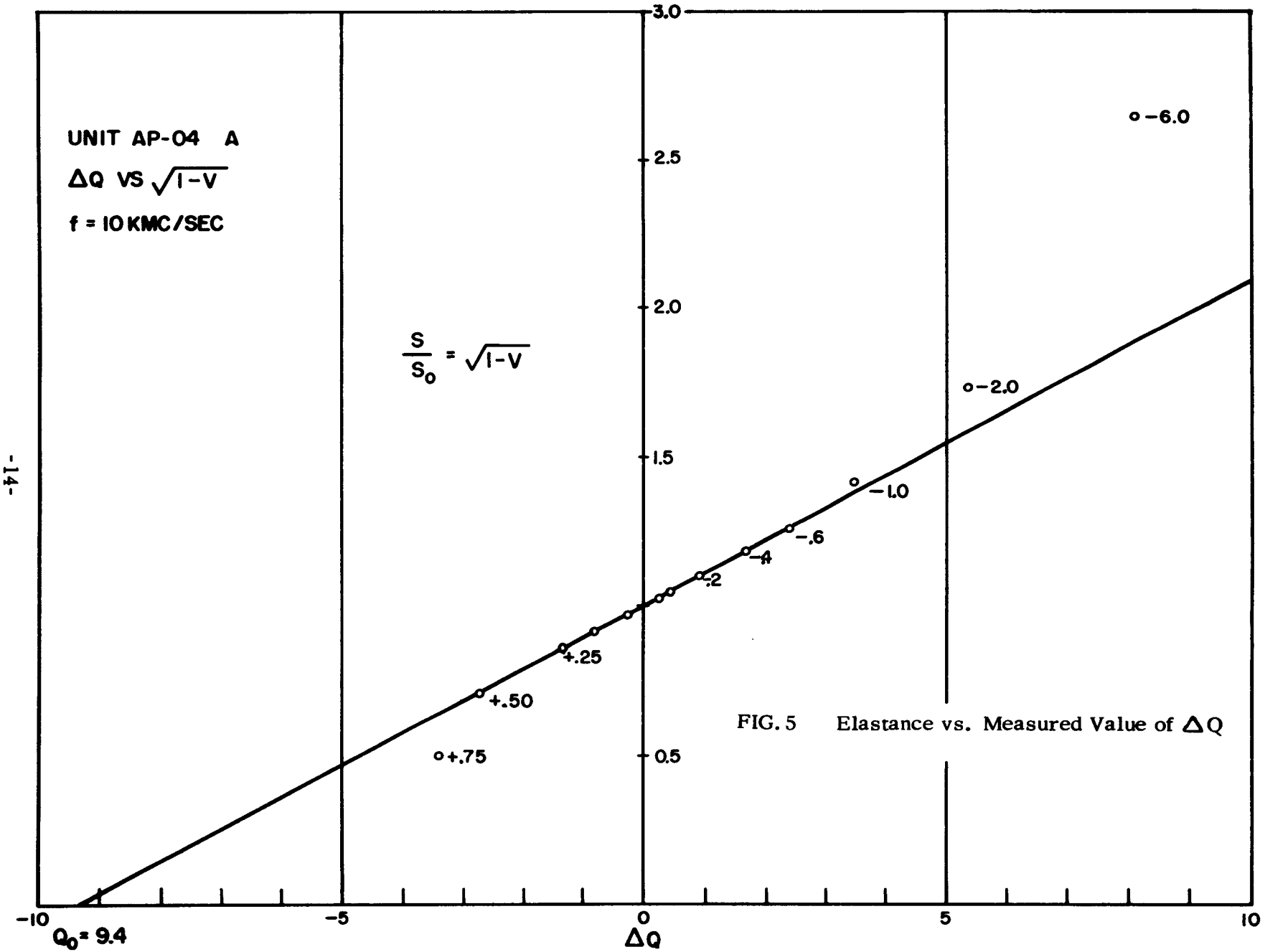


FIG. 5 Elastance vs. Measured Value of ΔQ

where $Q_o = 1/\omega C_{jo} R_s$. Now, if $V_2 = 0$ and $V_1 = \phi$, then:

$$\Delta Q(\phi, 0) = -Q_o \qquad (12)$$

In Fig. 5 the points around zero bias fall very close to a straight line, but at high reverse and high forward bias marked deviations can be seen. As mentioned above, a change of effective resistance is probably responsible for the error for the forward points, and measurement errors for the reverse bias points.

As a variation, Δ Q may also be calculated from the change in phase angle as the bias is varied. The normalized impedance of the diode is

$$Z = 1 + i\ \Delta Q(V_1, V_o) = re^{i\theta}$$

where $\Delta Q(V_1, V_o)$ is the change in Q when the voltage is changed from V_o to V.

Therefore,

$$\tan\theta = \Delta Q(V_1, V_o) \text{ or } \theta(V_1, V_o) = \tan^{-1}\Delta Q(V_1, V_o) \qquad (13)$$

The change in phase, $\Delta\theta$, for a change of voltage from V_1 to V_2, will be

$$\Delta\theta = \tan^{-1}\Delta Q(V_2, V_o) - \tan^{-1}\Delta Q(V_1, V_o) \qquad (14)$$

If we know ΔQ at one bias voltage and measure the change in phase angle going from bias V_1 to V_2, we can calculate $\Delta Q(V_2, V_o)$ as

$$\Delta Q(V_2, V_o) = \frac{\Delta Q(V_1, V_o) - \tan\Delta\theta}{1 + \Delta Q(V_1 V_o)\tan\Delta\theta} \qquad (15)$$

By using this procedure it is not necessary to measure large values of VSWR. $\Delta Q(V_1, V_o)$ can be established at some bias where the VSWR is not too large and can be accurately measured. Other values of ΔQ can then be determined simply by the change in phase angle of the minimum position.

Fig. 6 shows the results of plotting ΔQ vs. S where ΔQ has been determined in one case from a VSWR measurement (Eq. 9) and in the other from measurements of the change in phase angle $\Delta\theta$ (Eq. 15) along with the value of VSWR as determined at -0.4 bias.

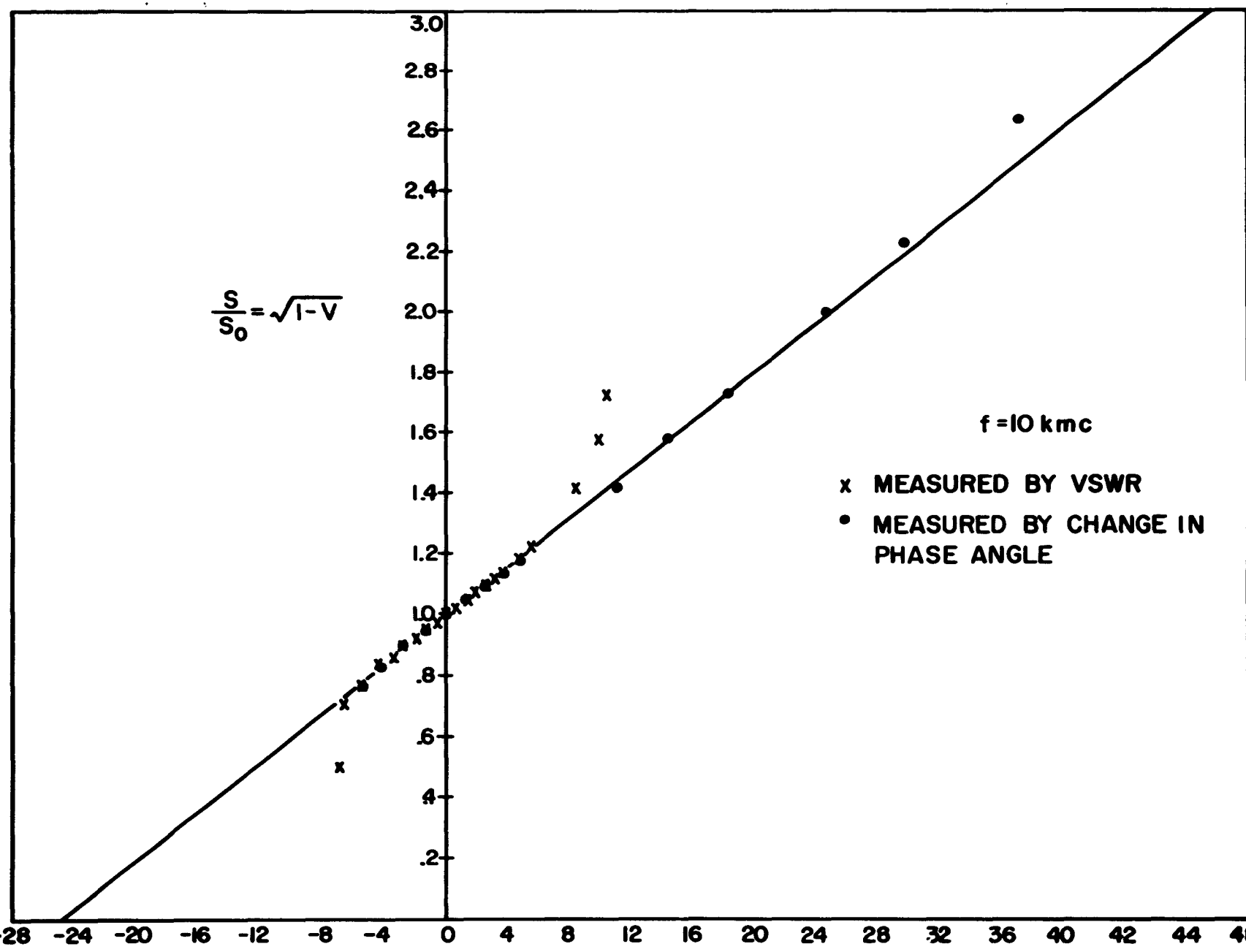


FIG. 6 Elastance vs. ΔQ as Determined from VSWR Measurements and from the Change in Phase Angle $\Delta \theta$

Some data has been taken by measuring ΔQ incrementally. The diode is matched to the slotted line at some value of bias and the bias changes are limited to produce a maximum VSWR of 10 db for each increment. The diode is rematched at each successive bias point, and cumulative losses are corrected by reciprocal measurements (measuring ΔQ for each increment for both increasing and decreasing bias conditions). The successive changes in ΔQ are then plotted against either the theoretical elastance variation ($S = S_0 (1-V/\phi)^{1/2}$ or the value measured on the 1 mc capacitance bridge. (Fig. 7). The disadvantage of this type of measurement is that any errors are cumulative. The following is the procedure that was used for the determination of varactor Q: Fig. 8 shows the experimental arrangement that was used. A nominal operating frequency of 10 KMC was used. Initially the rotary wave attenuator is set to zero and the level set attenuator is set around 15 to 20 db.

a. The crystal holder is replaced by a matched load and the E-H tuner is adjusted so that a minimum signal is seen at the standing wave amplifier when the switch is in position 1.

b. The matched load is replaced by the crystal holder with the varactor in place and the variable short is adjusted for a minimum reading.

c. The E-H tuner is then adjusted to give the minimum reflection.

d. The switch is moved to position 2 and the slotted line is used to check that the VSWR is close to one.

f. The bias on the varactor is changed and the VSWR and position of the minimum is read with the slotted line and rotary vane attenuator.

g. The data may now be presented on a Smith chart and ΔQ evaluated either by the VSWR (Eq. 9) or change in phase angle (Eq. 15).

At this point, a brief discussion of some of the relevant measurement difficulties might be in order. As previously mentioned the accurate measurement of large values of ΔQ is quite difficult. Only a relatively small power leakage or loss associated with the microwave holder will

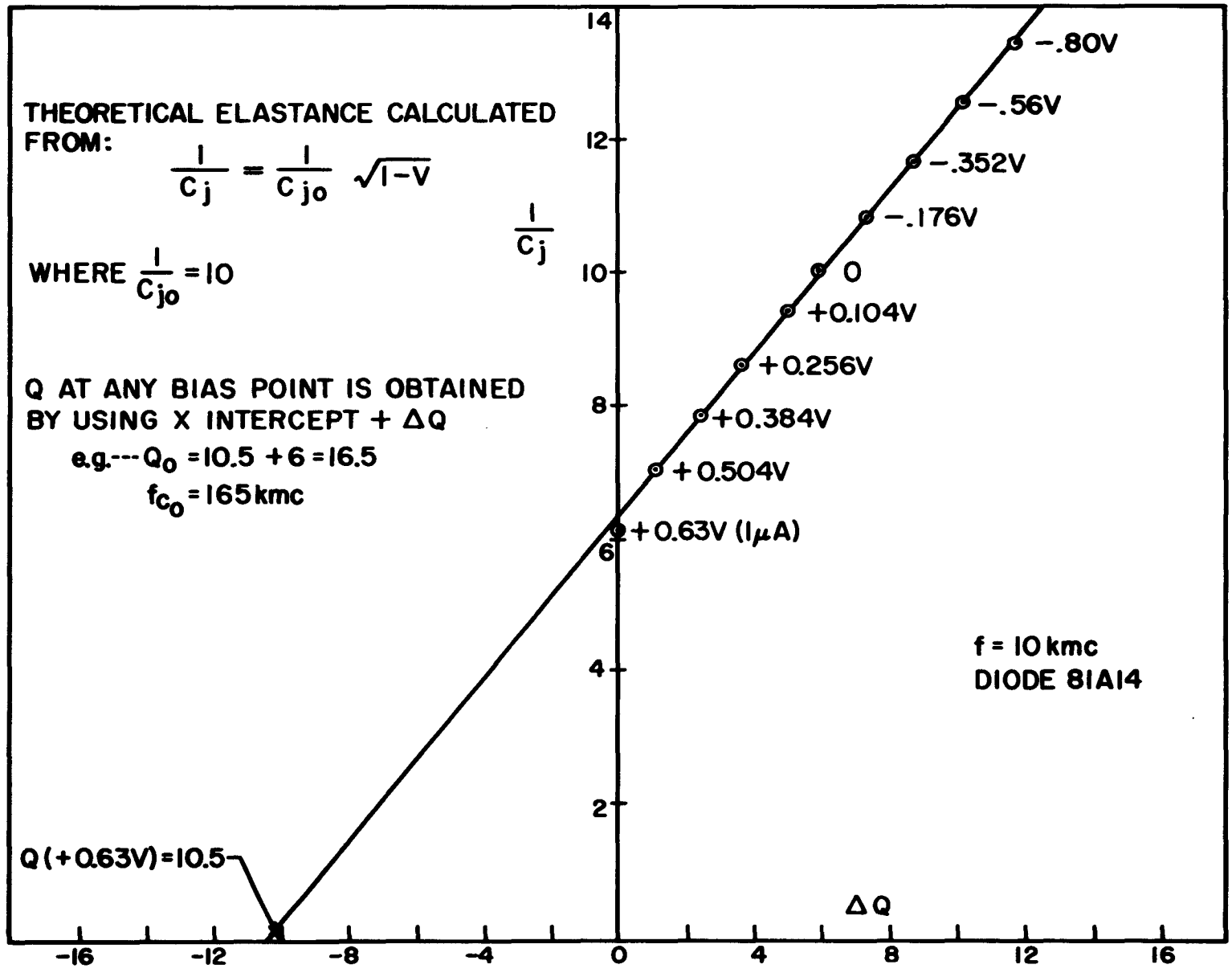


FIG. 7 Theoretical Elastance vs. Δ Q Measured by Incremental Method

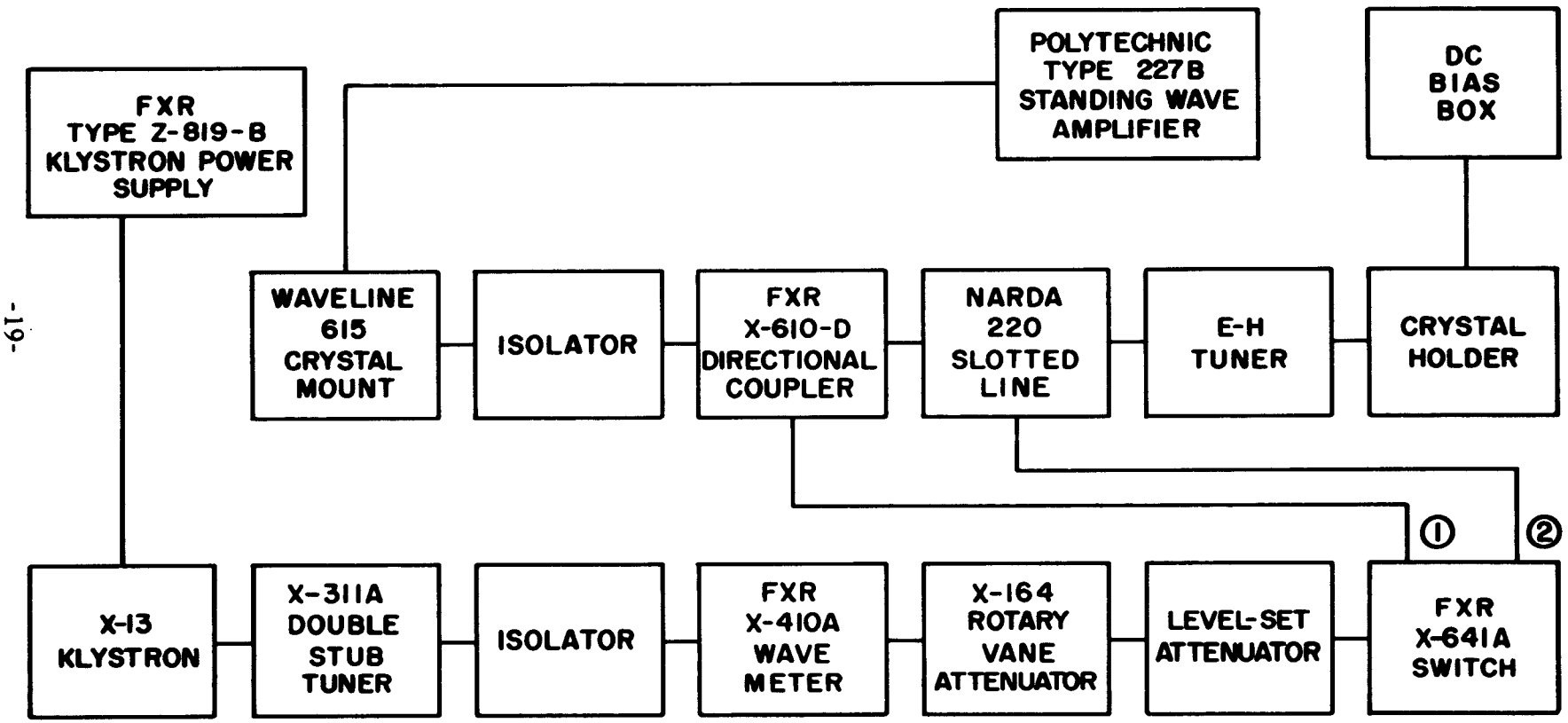


FIG. 8 BLOCK DIAGRAM OF MICROWAVE EQUIPMENT USED FOR Q MEASUREMENT

have a disastrous effect on the value of VSWR measured. To see this, consider a wave reflected from a boundary with reflection coefficient ρ (Fig. 9A). Before and after the reflection it undergoes a loss, $(1-\alpha)$. The VSWR will be:

$$\text{VSWR} = \frac{1 + \alpha^2 \rho}{1 - \alpha^2 \rho} \qquad (16)$$

If the loss is 3% ($\alpha = .97$), the measured value of the VSWR would be 29.8 db rather than the expected value of ∞ for reflection from a perfect short. Fig. 9 shows a plot of the value of VSWR that is measured against the actual VSWR for several values of α. It is for this reason that holder losses must be so small. For example, in Fig. 5 the point at -6 volts should have a VSWR = 47.5 db to fall on the line rather than VSWR = 36.6 that was measured. $\alpha = .99$ would account for this discrepancy.

The losses in the system must be kept very low in order to measure a high Q varactor accurately. For that matter, considerable care should be used in the design of parametric amplifiers and other varactor devices to reduce losses if the full potential of a good varactor is to be utilized.

If Q is determined from the measurement of phase, then the phase angle must be determined quite accurately at the point the reference value of ΔQ is measured. Any small error in $\Delta \theta$ becomes quite important when ΔQ is large. Also the evaluation of data is somewhat more tedious then for the VSWR method.

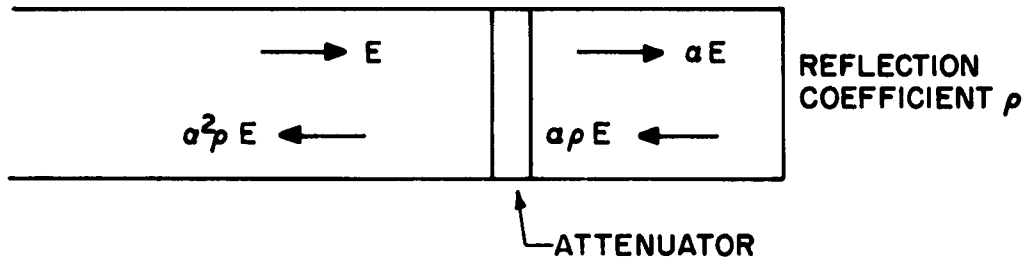


FIG. 9A Reflection from a Boundary with Attenuation

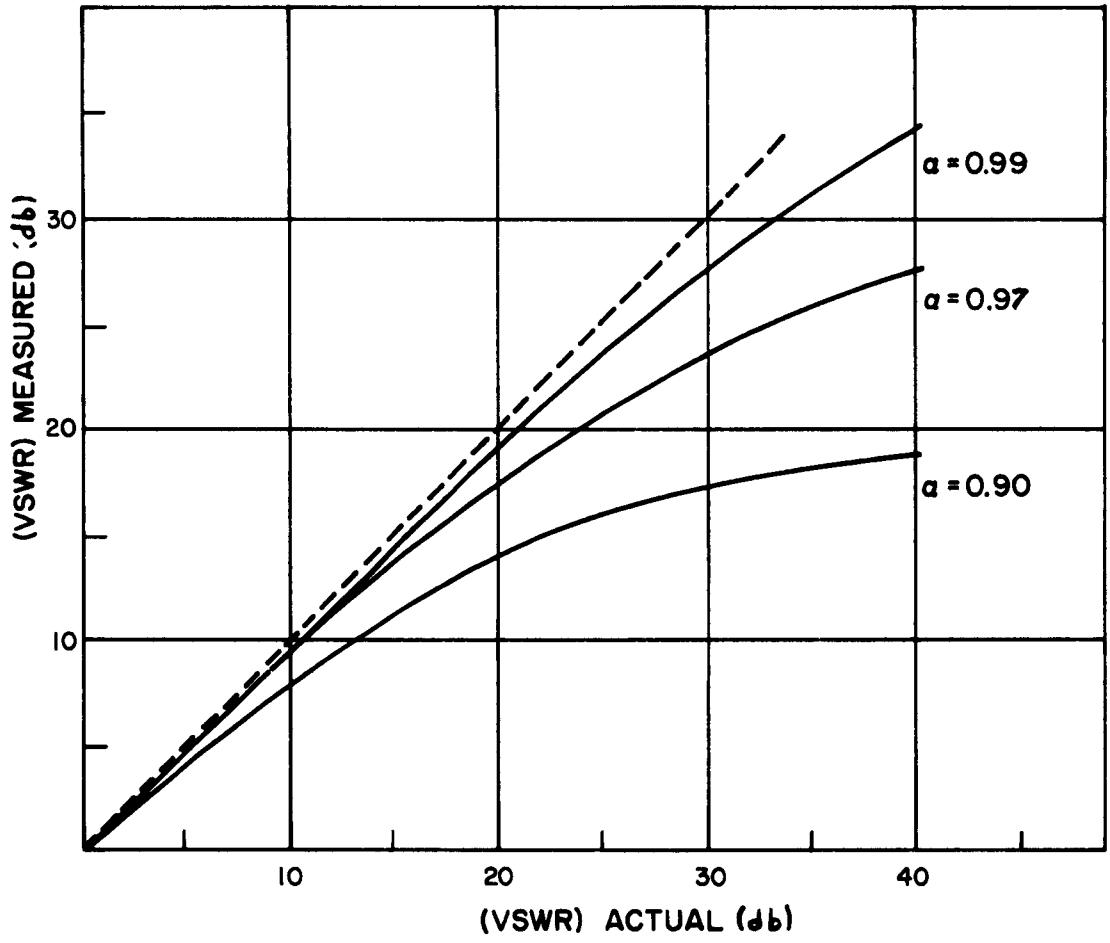


FIG. 9B Measured Value of VSWR vs. Actual VSWR with Various Values of Attenuation

3. Junction Capacity and Series Resistance

It has been observed empirically in the past that the junction capacity and Q of a varactor diode are closely related. In general, a diode with a high Q has a low junction capacity. In order to study this phenomena in a systematic fashion, a diode was constructed in a large crystal package. The pin to which the contact whisker is attached was advanced until it just made contact with the 0.002 Ω-cm GaAs chip. Complete measurements were then made of the capacity at 1 mc and ΔQ at 10 KMC for bias voltages between +0.50 and -3.0 volts. The contact whisker was then forced against the GaAs chip slightly harder. The increase in pressure deforms the point of the contact whisker so that a larger area of contact and, therefore, a larger capacity result. This procedure was carried out five more times with detailed measurements of capacity and Q being made each time. Fig. 10 shows $C_T(V)$ versus $(1-V/\phi)^{-1/2}$ where $\phi = 1.3$ volts for this set of measurements. Table III shows Q_o, C_{jo}, and R_s for various steps. R_s was computed from equation (1). Fig. 11 shows $1/C_o$ versus R_s. R_s approaches a constant value of approximately 1.5Ω as the capacity increases. It is surprising that R_s should have as a limit such a large constant value. Roughly, one would expect that R_s^2 and $1/C_{jo}$ would be proportional to each other. C_{jo} will be proportional to the contact area. If R_s is determined only by the spreading resistance, then

$$R_s = \rho/2\pi r_o \tag{17}$$

Therefore, R_s^{-2} would also be proportional to area. As is quite obvious, this is not the case, but rather in addition to the spreading resistance, there is a series resistance of approximately 1.5 ohms.

Another interesting comparison to make is that of R_s as determined from microwave measurements and the value of R_s calculated from the spreading resistance. The capacity per unit area has been determined from large area junctions as a function of resistance for GaAs. Using the 1 mc capacity measurements the area of the junction can be estimated and assuming a spherical junction the spreading resistance can be calculated (Table III). The spreading resistance is too small by a factor of ten to account for the measured microwave resistance.

FIG. 10 Total Capacity vs. $(1 - V/\phi)^{-1/2}$

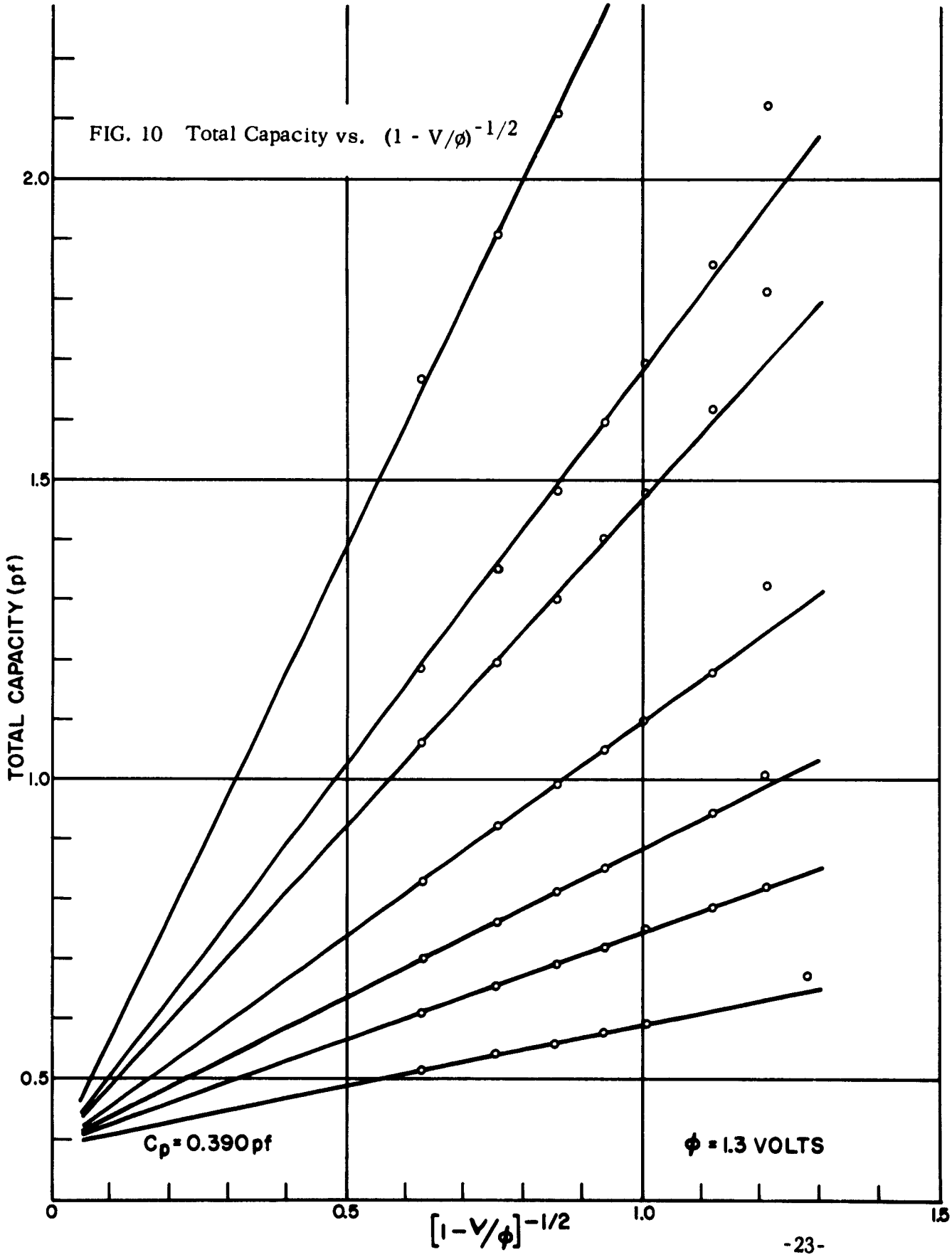


TABLE III

Junction Capacity and Q_o of a 0.002 Ω-cm GaAs Varactor as a Function of Contact Area

$$R_s = \frac{1}{Q_o C_{jo} \omega} \qquad R_s = \left(2\frac{\pi}{A}\right)^{1/2} \rho$$

	C_{jo} (pf.)	Q_o	$(R_s)_m$ (Ω)	Area (cm^2)	$(R_s)_c$ (Ω)
1	0.1996	18.0	4.43	2.17×10^{-6}	.54
2	0.3637	16.3	2.67	3.94	.40
3	0.494	13.7	2.37	5.36	.33
4	0.704	10.8	2.09	7.65	.29
5	1.088	8.20	1.78	11.8	.23
6	1.304	6.91	1.76	14.2	.21
7	2.069	4.63	1.66	22.5	.17

The junction capacity, C_{jo}; Q_o; and resistance, $(R_s)_m$, were determined by microwave measurements. The area was determined from the known variation of capacity per unit area with resistivity for P-N junctions. $(R_s)_c$ was calculated from the area and resistivity (.002 Ω-cm).

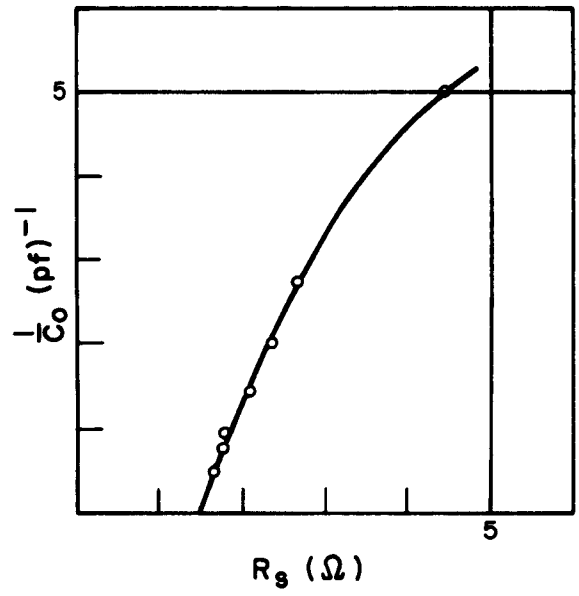


FIG. 11 Reciprocal of the Junction Capacity vs. R_s

The source of this additional resistance was not isolated but several possibilities are:

a. Resistance of the contact wire, especially that associated with the point or poor contact of the semiconductor to its post;

b. A thin layer of some relatively high resistance material between the wire and the junction, such as an oxide layer;

c. A piezoresistive effect caused by the large strain at the junction;

d. Contribution to the losses from dielectric relaxation.

Some inconclusive investigations have been made of possibility a. When two packages with no semiconductor were assembled, resistances of 1.3 and 1.9 ohms were obtained. Initially, the sharp point was pushed forward until it just made contact and the resistance measured. The wire was advanced in one sample and the resistance decreased to 0.3 ohms. Using a rounded contact wire, resistances of 0.02 and 0.04 ohms were obtained. However, when the varactor diodes were constructed using a rounded wire, no marked improvement in their properties was noted.

B. PACKAGE DEVELOPMENT

The package being used at the start of this program consisted essentially of a cylindrical ceramic tube having gold-plated end plugs (Fig. 12A). The overall dimensions of this "pill" were approximately 0.25" dia. x 0.125" long. One plug had the GaAs chip mounted on it, and the other had a phosphor bronze C-shaped wire spring with a pointed end to make contact to the chip. This package and device structure have been used to test epitaxial GaAs.

The program of development has divided its attention between the package as such, and the internal construction of the contacting arrangement. Since the original package has a capacitance of about 0.2 pf, it was necessary to reduce this substantially so as to make it consistent with

the low values of junction capacitance of about 0.1 - 0.3 pf. A logical choice of material to substitute for the alumina-based ceramic was quartz, and this, indeed, has enabled the package capacitance to be reduced to about .07 pf. (The wall-thickness of the quartz can probably be reduced slightly to give an even lower value of package capacitance, but the mechanical strength becomes a problem). Table IV shows the values of capacitance of empty pill packages as a function of geometry and ceramic. The values agree very well with those calculated from the well-known formula relating capacitance to the area and spacing of the metal plates, and the geometry and dielectric constant of the ceramic. Because of stray capacitative effects when a junction is inside the pill, a somewhat higher package capacity is observed. This amounts to typically 0.02 to 0.05 pf.

The heart of the varactor comprises the GaAs chip and the whisker which makes contact to it. In order to satisfy the electrical requirements of a sharp junction and of a controlled junction capacitance, the whisker must be made of a suitable material and have a proper geometry at the point. Further, to insure stability of operation under differing conditions of ambient (temperature, vibration, etc.), there must be allowance for expansion and contraction of the whole assembly. Since it has been found that the whisker must contain copper in order to yield the required electrical characteristics, and since several copper-containing alloys are reasonable spring materials, it has been common practice to use a C-bend spring of phosphor bronze or beryllium copper as the combined mechanical and electrical assembly. However, the distributed capacitance and inductance, and the lack of axial symmetry of this construction, made it less than ideal at high frequencies. In order to examine the possibilities of alternate methods of construction, a study was made of the detailed behavior of the C-springs.

By using a projection microscope (31.25 X), the spring constant and motion of standard C-springs were measured. It was found that:

1. Some transverse motion of the point across the surface of the chip occurs during the squeezing operation:
2. The spring constant varies considerably from whisker to whisker.

TABLE IV

Package Capacitance as a Function of Dielectric Material

Material	Dimensions O.D." x L" x I.D"	Capacitance picofarads
Alumina	.093 x .060 x .046	.19 - .20
Alumina	.105 x .070 x .070	.130 - .135
Alumina	.105 x .060 x .070	.150 - .170
Alumina	.105 x .150 x .070	.09 - .11
Sapphire (Syn.)	.093 x .047 x .060	.160 - .200
Quartz	.086 x .060 x .060	.07 - .08
Quartz	.116 x .060 x .065	.102 - .112

As a result of these findings, a completely new package design was undertaken, using a bellows assembly in place of the C-bend.

The expected advantages of the new construction, shown in Fig. 13 are as follows:

a. Accurate reproducibility of the spring action;

b. Complete axial symmetry of the device;

c. Much reduced package inductance; although the package capacity is increased by roughly 0.05 pf;

d. Freedom of choice of the actual junction forming material, since this does not also have to provide the spring action;

A number of diodes were constructed with this configuration, but unfortunately none with a high Q were obtained. The problem is felt to be just a matter of developing the proper fabrication techniques to take advantage of this type of geometry.

Several other types of packages have been used besides the standard "pill". These are illustrated in Figs. 12A through 12E. By using a longer ceramic piece (Fig. 12B) the package capacitance is greatly reduced, but because of the longer C-spring and metal pins the inductance is somewhat larger. Fig. 12C shows a type of construction in which the length of the metal plugs has been increased. The GaAs chip was mounted on one pin and the contact wire on another, thus making assembly quite easy. The metal plugs were kovar and were soldered to the ceramic. Fig. 12D illustrates a type in which a quartz spacer was used to reduce the package capacitance. The standard microwave package (Fig. 12E) is the easiest type to assemble and gives more consistent and reproducible results than the other types. For this reason, it was used a good deal in the evaluation of various materials.

Normally, the end plugs of the packages are held in place with epoxy or soldered, but several varactors were constructed by screwing the end pieces into the ceramic. Some of these units gave an extremely high Q (Fig. 6), which indicates the epoxy makes some contribution to the losses. At breakdown, f_c = 750 KMC for the diode shown in Fig. 6.

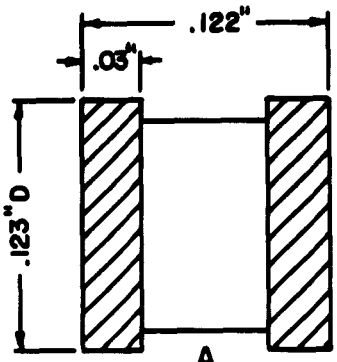


FIG. 12A Outline of Standard Pill

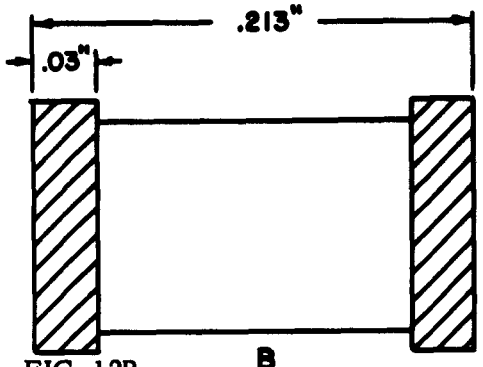


FIG. 12B Outline of Pill with Long Ceramic

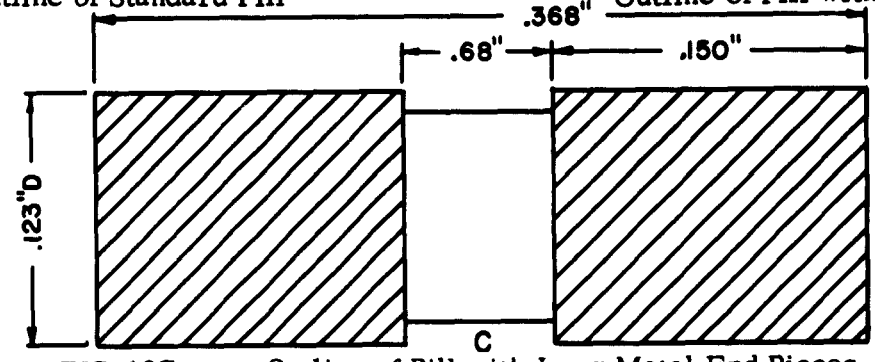


FIG. 12C Outline of Pill with Long Metal End Pieces

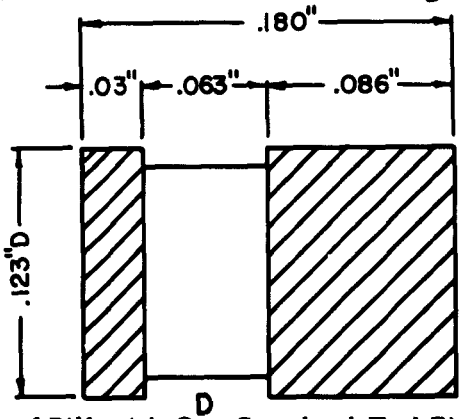


FIG. 12D Outline of Pill with One Standard End Piece and One Long End Piece

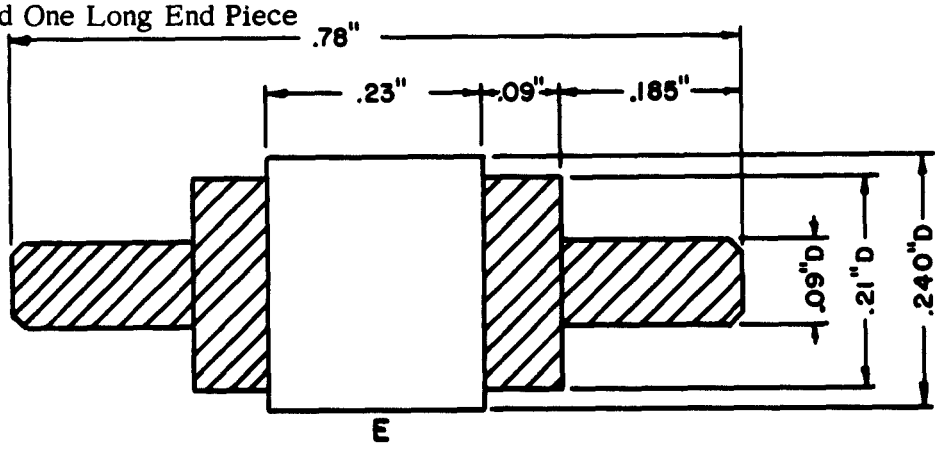


FIG. 12E Outline of Microwave Cartridge

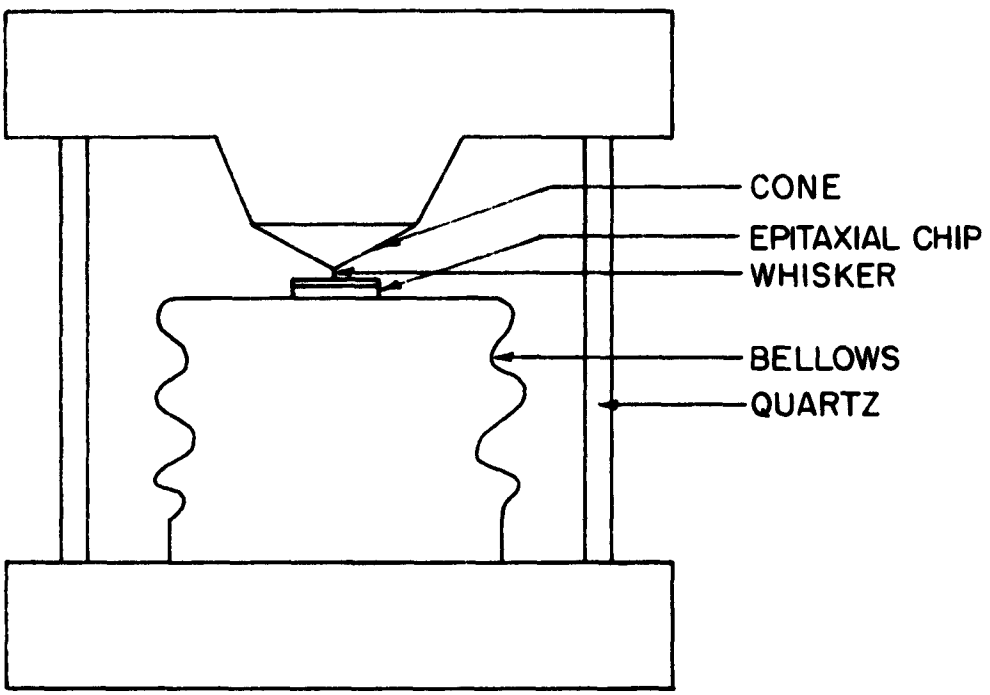


FIG. 13 BELLOWS CONSTRUCTION

In Table V the properties of the GaAs diodes which have been submitted are given. Among the properties given are the cut-off frequency at -4 volts and the cut-off calculated at the breakdown voltage (voltage at which the reverse current equals 10 μamp). The total capacity at zero bias is given and also the type of package is indicated.

TABLE V

Data on Submitted Diodes

Diode No.	V_b (Volts)	V_f (Volts)	f_c (-4V) (KMC)	f_c (V_b) (KMC)	C_T(0) (pf)	Type
1	11.0	1.08	198	307	.380	1
2	8.5	1.02	309	426	.322	2
3	7.0	0.96	217	274	.710	1
4	11.3	1.15	223	350	.329	3
5	6.0	0.95	279	331	.575	4
6	6.0	1.30	223	264	.408	1
7	6.0	1.15	93	110	.510	4
8	9.5	1.45	148	214	.280	1
9	7.0	1.31	211	269	.460	2
10	6.0	.85	323	384	.450	5
11	9.6	.86	334	486	.438	6
12	10.4	.93	379	575	.532	6
13	10.0	.90	143	212	.330	3
14	3.0	.80	--	121	.791	7
15	8.0	1.21	260	349	.764	6
16.	10.0	1.25	135	200	.280	1

V_b - Voltage required for 10 μamp current in reverse.
V_f - Voltage " " 3 ma " " forward.
C_T (0) - total capacity including junction and package.
f_c (-4V) - cutoff frequency at -4 volts.
f_c(V_b) - " " at V_b.

Type 1 - thin walled alumina pill, Fig.12A($C_p \approx 0.22$pf).
Type 2 - long, thin walled alumina pill, Fig.12B($C_p \approx 0.09$ pf).
Type 3 - standard pill, Fig.12A($C_p \approx 0.22$ pf).
Type 4 - soldered case, Fig.12C($C_p \approx 0.22$ pf).
Type 5 - clear quartz case, Fig.12D($C_p \approx 0.15$ pf)
Type 6 - standard microwave cartridge, Fig.12E($C_p \approx 0.39$ pf).
Type 7 - pill with bellows in quartz Fig.12A($C_p \approx 0.15$ pf).

III. MATERIALS RESEARCH

A. INTRODUCTION

The major aim of this program has been to explore the feasibility of using high energy gap materials in the construction of varactor diodes. To this end, two distinct materials areas have been explored. On the one hand, a basic study has been carried out in order to substantiate the hypothesis that materials of higher energy gap would provide for a higher Q factor than materials of lower energy gap. This study essentially involved a determination of the voltage breakdown and capacitance of large-area defined-geometry abrupt junctions as a function of resistivity and carrier concentration. The adjunct materials program was involved essentially with the preparation of highly perfect epitaxial single crystal films of gallium arsenide and gallium phosphide. In this case, the basic desire was to prepare material such as gallium phosphide in a suitable configuration for measurement of its high frequency characteristics (the point contact diode configuration was employed).

B. FABRICATION OF DEFINED- GEOMETRY LARGE-AREA ABRUPT JUNCTIONS OF SEMICONDUCTING COMPOUNDS

A Figure of Merit of varactor diodes is the total amount of energy which can be stored and released in a given cycle. This stored energy is given by:

$$Q(f) = \frac{1}{R_s C 2\pi f} \tag{18}$$

where f is the frequency of the signal, R_s is the series resistance between the P-N junction and external leads and C is the capacitance of the P-N junction. The maximum Q(f) is obtained when the product $R_s C$ is a minimum. Also, the maximum Q(f) which can be utilized by a device is stored when the applied voltage is highest, that voltage, V_{max}, being given by the expression:

$$V_{max} = X V_g + V_b$$

where

V_g = energy gap
V_b = breakdown voltage
X = a factor less than unity

The aim of this study was to investigate the validity of the hypothesis that higher values of Q(f) are obtainable with materials of higher energy gap. To accomplish this,well-defined geometry large-area abrupt P^{++} on N junctions were fabricated. If our hypothesis is correct, the R_sC product normallized to equal V_b should decrease with increasing energy gap. The P^{++} on N structure was utilized since the high conductivity P-layer contributes little to the R_s or V_b of the junction. Normal alloying and regrowth and the Travelling Solvent Method of Crystal Growth have been used to fabricate the P^{++} on N structures.

1. GaAs

(a) Alloying and Regrowth

The process of alloying and regrowth has been used to produce P^{++} on N structures of GaAs. This procedure produced extremely sharp large-area junctions. The electrical properties of rectifying junctions such as V_b and C may often be merely manifestations of improper junction fabrication. Therefore, great care was taken in the preparation of the P^{++} on N structures. The procedure used to prepare the desired junctions is reported below:

(1) A slice of GaAs (approximately 50 mils thick x 250 mils dia.) of the desired resistivity and type was placed in a quartz tube 255 mils in dia. An alloy of 99% Ga + 1% Ge was then placed on the surface of the slice. All materials were carefully etched and cleaned before assembly.

(2) This assembly was then mounted on a carbon pedestal directly below a carbon strip radiation heater. The entire assembly was then placed in a bell jar which had suitable ports to allow both evacuation and entrance of inert gas.

(3) Before the heating cycle was initiated, the system was evacuated and flushed for two hours.

(4) The radiation heater was then energized. The temperature, as measured by a thermocouple in contact with the bottom of the slice, was increased to 700°C in 15 minutes.

(5) After holding at 700°C for 15 minutes, the temperature

was decreased at a rate of 40°C per hour. The system was cooled rapidly from 200°C to room temperature.

(6) The sample was then removed from the system and placed in warm HCl to dissolve the excess Ga on the surface. A slight amount of precipitated GaAs was normally present in the liquid Ga. A regrown region at least 15 mils thick was produced in all cases.

(7) After removal of the excess Ga, the large samples were diced into cylindrical samples 40 mils in dia. on an ultrasonic vibration grinder. A cylindrical sample stained in a solution of 3 parts H_2O : 1 part HNO_3 : 1 drop HF, is shown in Fig. 14. The P regrown region may be seen as the thin darkly stained region.

(8) After etching the dice in 3 HCl : 1 HNO_3 for a few seconds, the ohmic contacts were prepared. The "P" type contact was made by melting an alloy of 1 Au : 1 Ga : 1 Ge onto the surface of the chip at 800°C in a hydrogen atmosphere. The "N" type ohmic contact was produced by alloying with a Au : 20% Sn preform (already attached to a kovar pin) in hydrogen at 550°C. The entire assembly may be seen in Fig. 15.

(9) This assembly was then etched in a 1 HNO_3 + 3 HCl solution until a sharp breakdown and low leakage current were observed.

(10) The entire assembly was then mounted in the package shown.

NOTE: Solvent zones of Ga-Ge alloys of germanium concentration greater than 1% Ge gave poor results. A great deal of work was done to obtain a suitable ohmic contact to the P-type layer. Contact materials such as In, In-Zn, Au-2% Zn, Ga-Ge, and Au-Zn-Ge, were studied. The only successful alloy composition was found to be an alloy of equal proportions by weight of Au-Ga-Ge.

(b) Travelling Solvent Method (TSM)

P^{++}-N junctions have been fabricated by TSM. In this technique, a zone of liquid Ga, doped with the appropriate P-type carrier is sandwiched between two slices of N-type GaAs. A temperature gradient is then impressed upon the sample by heating the top surface by radiation and cooling the bottom by convection. GaAs dissolves in the liquid gallium zone at

FIG. 14 Cylindrical P^{++} on N Chip of GaAs (junction stained out in 3 H_2O:1HNO_3: 1 drop HF)

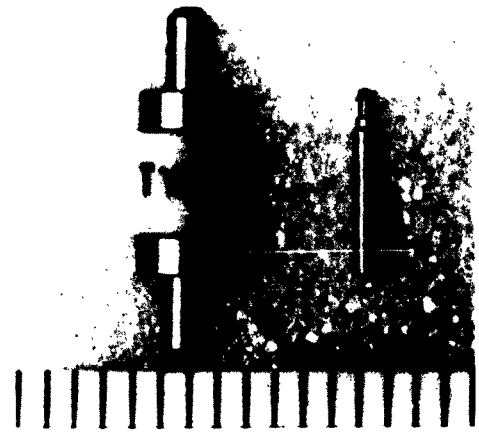


Fig. 15 Diode Assembly

the upper surface (higher temperature), and redeposits on the bottom surface (lower temperature) and the solvent zone is thus made to move up through the top slice. This is illustrated in Fig. 16. During this process, the top slice is doped with the impurity element, the amount of doping being determined by the distribution coefficient of the impurity between gallium and solid GaAs.

Three P-type dopants, zinc, cadmium, and germanium, were investigated. Cadmium, which has a K_{GaAs} equal to 0.2 at the melting point of GaAs, was initially used as a dopant. The fabrication of the GaAs-Ga 1% Cd-GaAs sandwich was accomplished by immersing the two GaAs slices in a melt of Ga + 1% Cd. By means of a micrometer mechanism, the upper slice was raised 0.001 inches, thereby allowing a similar thickness of Ga + 1% Cd to complete this sandwich structure. Since Cd is extremely volatile (P_{Cd} = 5 mm) at the Ga-GaAs wetting temperature (500°C), the predetermined weight of Cd was dropped into the liquid Ga just prior to the GaAs immersion. After careful microscopic examination of the first junction, it was found that the zone had broken up and a movement of approximately 20 mils had occurred in a few sections through the sandwich. Improper wetting apparently caused the limited movement. In the second run, using a 1% Cd solvent zone, movement occurred across the entire Ga-GaAs interface, as can be seen in Fig. 17; however, a second phase formed in the regrown crystal. The third Cd-rich regrown crystal is shown in Fig. 18. The liquid Ga zone can be seen as a black area adjacent to the remaining section of the top slice. An attempt to determine the conductivity type of the variously stained regions using a hot probe, met with only limited success. Since the hot probe technique is relatively insensitive to variations in conductivity in GaAs, the only information obtainable was that the regrown region was definitely P-type.

Since Cd volatized rapidly from the Ga melt and also tended to form a second phase on regrowth, Zn, which has a higher distribution coefficient, $0.97 > K_{GaAs} > 0.2$, was studied as a possible P-type dopant. Extremely sharp junctions were obtained as shown in Fig. 19 (magnified x 2000) and Fig. 20 after staining to show a change in conductivity type. The resultant structure, however, exhibited poor rectification characteristics. Successful results were obtained using Ge as a doping constituent in the liquid Ga zone.

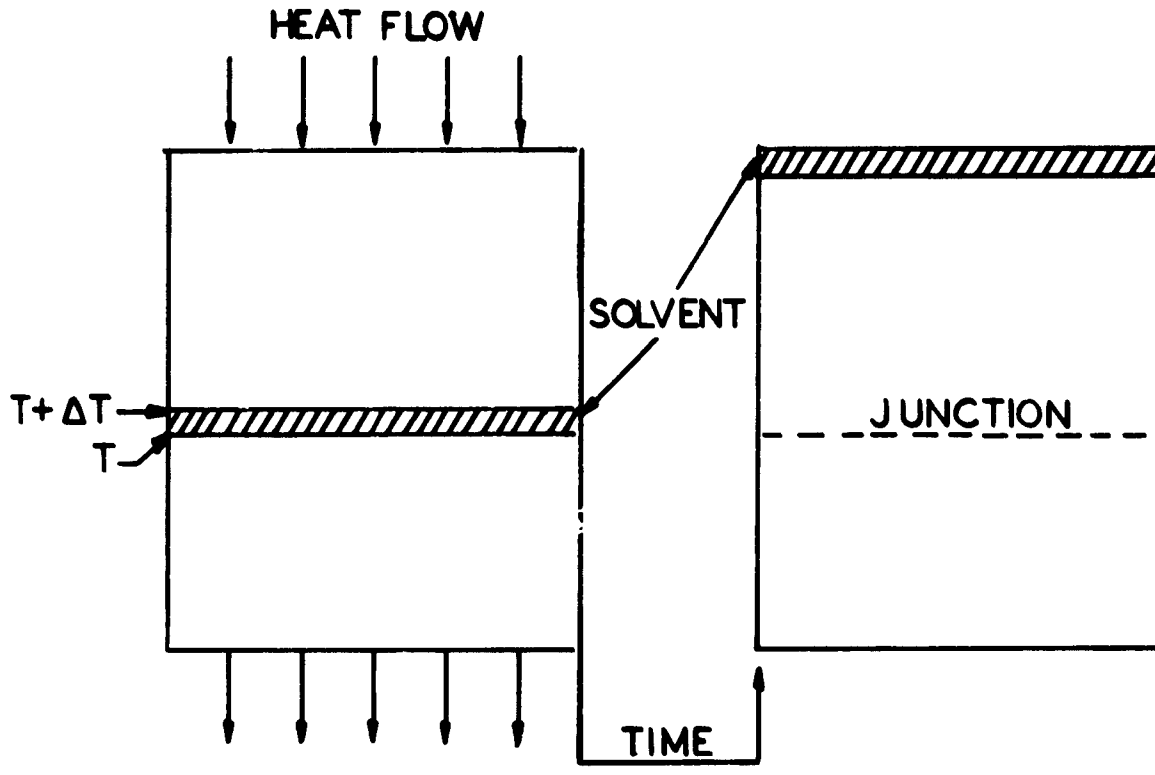


FIG. 16 The Travelling Solvent Method

FIG. 17 Cross-Section of Cd-rich GaAs Regrown Crystal Showing Formation of a Second Phase (stained in 1:1 HNO_3:H_2O)

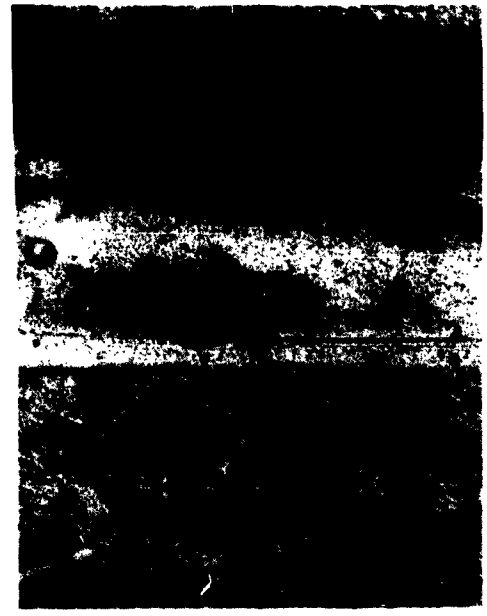


FIG. 18 Cross-Section of Cd-rich GaAs Regrown Crystal Showing Zone Movement. Liquid Ga Zone May be Seen Near the Top of Sandwich. (stained in 1 HNO_3:1 H_2O) 100X

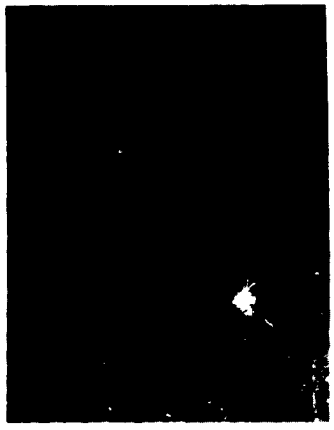


FIG. 19 Junction Between Zn-rich Regrown GaAs and Original Crystal (etched in CP_4) 2000X

FIG. 20 GaAs (Zn-doped) P^{++}, on N Structure Fabricated by TSM (stained in 1:1 HNO_3:H_2O) 200 X

Crystals grown by TSM from a 2% Ge-Ga zone were extremely high conductivity P-type. A photomicrograph of the P^{++} on N structure produced by TSM is given in Fig. 21. The P-layer stained out in a solution of 1 part HNO_3 + 3 parts H_2O + 1 drop of HF. Diodes were produced from TSM grown structures in the same manner as reported for the alloy grown structures.

(c) Electrical Evaluation of P^{++} on N Junctions

(i) Voltage Breakdown as a Function of Resistivity

Detailed measurements of the capacitance of the junctions as a function of the bias voltage confirmed the fact that the junctions were extremely abrupt. The theoretical dependence of capacitance on voltage is given by the relation:

$$C_v = \frac{C_o}{(1 - V/\phi)^n} \qquad (19)$$

where C_o is the junction capacitance of zero bias, C_v that at a bias voltage V (positive forward bias), and ϕ is the built-in junction potential (flatband position is achieved as V approaches ϕ; C_j then approaches infinity) and n has the value of 1/2 for abrupt and 1/3 for a graded junction according to simple P-N junction theory. In all the diodes measured, the best fit to date was always achieved by setting n equal to 0.50. Accordingly, we define the junctions made by the above techniques as abrupt. Fig. 22 shows the capacitance as a function of bias for a typical diode. As can be seen, the diode adheres very closely to a square law capacitance-voltage dependence. The current-voltage characteristic of a typical GaAs P^{++} on N junction is given in Fig. 23. Forward current may be characterized by the relationship:

$$I = I_o \exp^{(eV/\eta KT)} \qquad (20)$$

where η is equal to 2. The value of 2 denotes non-linear carrier recombination. The electrical properties of P^{++} on N GaAs junctions may be found in Table VI. Fig. 24 shows the voltage breakdown at 25°C as a function of resistivity. For comparison, data on Zn-diffused GaAs junctions and abrupt Si junctions are shown. Each experimental point represents measurements

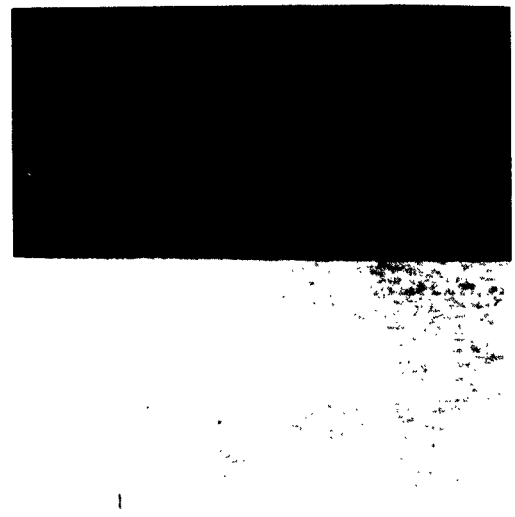


FIG. 21 P^{++} on N Structure (stained in 1 HNO_3:3 H_2O:1 HF) 900 X

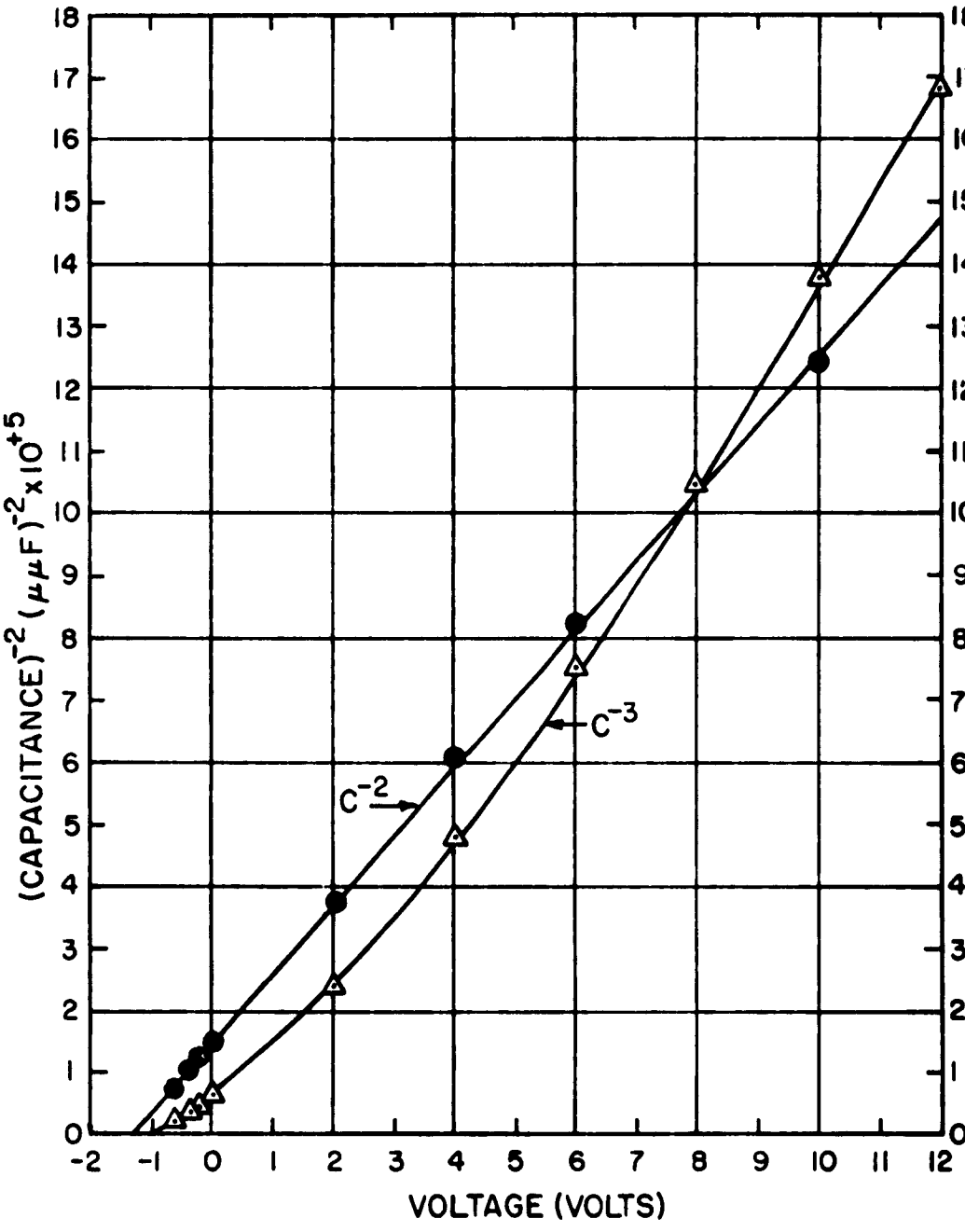


FIG. 22 Square Law Behavior of GaAs P^{++} on N Large Area Junction

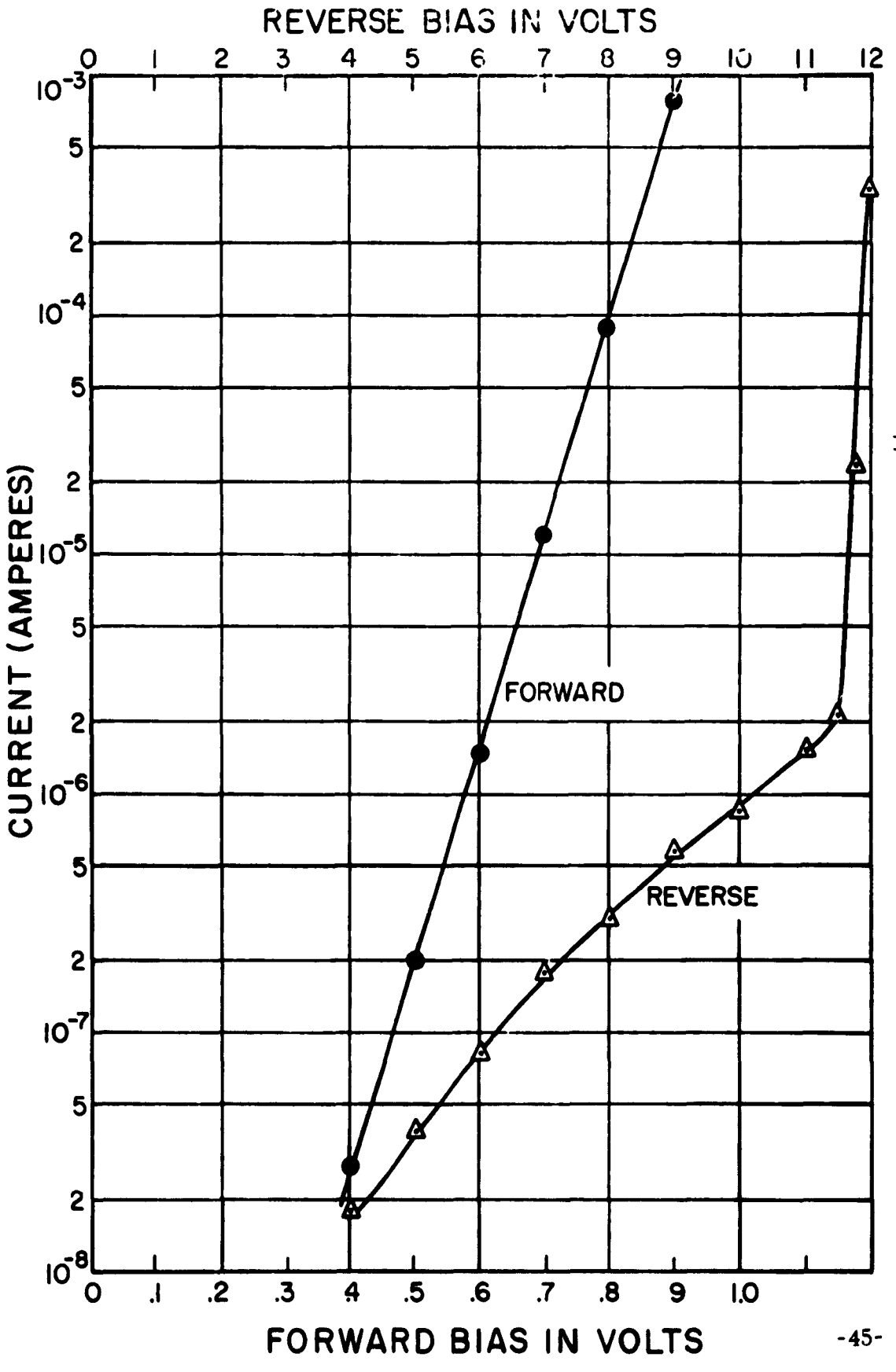


FIG. 23 I-V Characteristic of GaAs P^{++} on N Large Area Junction

TABLE VI

Electrical Properties of P^{++} on N GaAs

Sharp Junctions

Sample No.	P (ohm-cm)	V_B (volts)	C (at -1 volt) (mmf)	V_F (at 1 ma) (volts)	n_F (2 log I/av)
3A4	0.045	15.5	195	0.95	-
6A2	0.045	12.5	-	0.90	3.39
6B2	0.045	14.0	208	1.15	-
7A1	0.00062	1.1	-	1.0	3.30
7A2	0.00062	0.4	-	0.9	3.22
7A3	0.00062	1.1	803	0.9	3.17
7A4	0.00062	1.0	-	0.9	3.38
7A5	0.00062	1.0	-	0.9	3.08
7B1	0.00062	1.2	908	1.1	-
7B2	0.00062	1.4	-	0.9	3.08
7B3	0.00062	1.5	-	0.9	2.95
10B1	0.01	10.5	339	1.0	2.12
10B2	0.01	10.5	372	0.9	2.04
10B3	0.01	11.5	282	0.9	1.95
10A1	0.01	11.8	-	1.0	-
10A2	0.01	11.5	274	1.0	2.30
22-1	0.008	8.0	451	1.0	1.85
22-2	0.008	8.5	-	0.85	2.10
28-5	0.0032	5.2	-	0.65	-
28-6	0.0032	5.9	335	0.65	1.61
28-7	0.0032	6.5	233	0.70	1.61

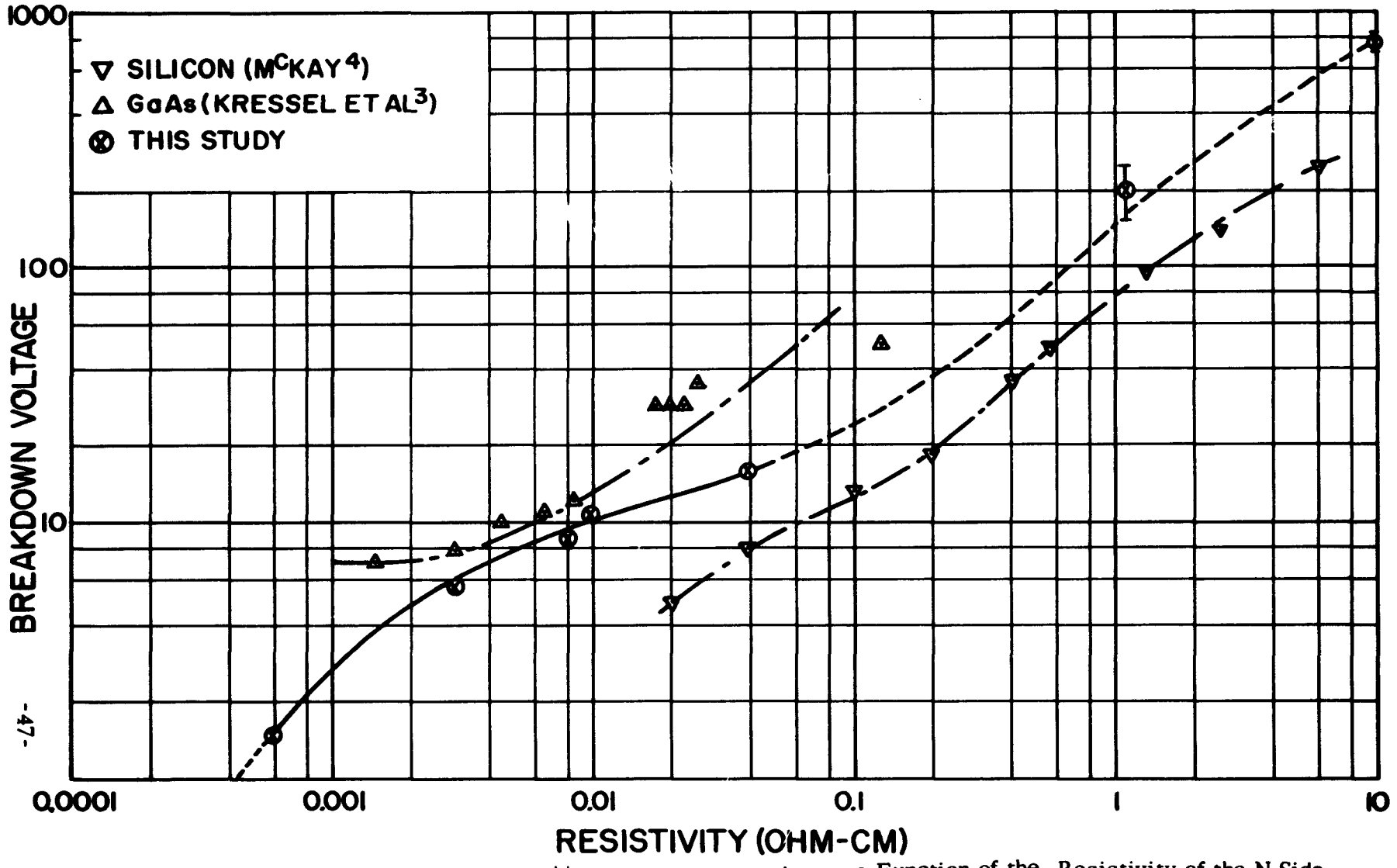


FIG. 24 The Breakdown Voltage of GaAs P^{++} on N Abrupt Junctions as a Function of the Resistivity of the N Side

on at least 10 diodes. In all cases of resistivities other than 1 Ω-cm and 10 Ω-cm, the breakdown voltages varied less than 0.5 volts from diode to diode made from material of a given resistivity. In the case of the high resistivity material, sharp breakdowns were exhibited; however, forward characteristics were extremely poor. Breakdown was defined as the voltage at which the reverse current of 20 μA was observed. It was noted that diodes prepared by regrowth on the (111)A-face (Ga), and those regrown on the (111)B-face (As), showed identical breakdown voltages for a given resistivity. This observation is in contradiction with the prediction of Minamoto[1] derived from InSb diodes. Fig. 24 shows clearly that for a given resistivity zinc diffused GaAs diodes have a higher breakdown voltage than abrupt alloyed GaAs diodes, which in turn is higher than that of Si diodes. It is well known that a graded junction exhibits a higher breakdown voltage than an abrupt one for a given resistivity. Accordingly, we conclude that the Zn-diffused diodes reported have indeed graded junctions, although the authors described them as nearly abrupt. Fig. 25 is a plot of the experimental data of breakdown voltage vs. carrier concentration for our diodes and for abrupt Si diodes. Also shown is a curve given by Kressel[2] and others for diffused GaAs diodes. The remarkable similarity between our data and that for Si may be coincidental since Ge shows a quite different behavior. The higher values of breakdown shown by GaAs compared with Si of the same resistivity follow directly from the higher carrier mobility in GaAs. The breakdown voltage, V_b, vs. carrier concentration, N, follows the relation:

$$V_b = 10'' N^{-0.58} \tag{21}$$

The GaAs abrupt junction data follows this relation from 700 V down to 1.5 V, whereas the Si data begins to deviate at about 7 V and lower. Miller[3] describes this deviation at high values of N for Si to the tendency towards saturation of the ionization rates at very high field strength. Although a deviation of the same type is shown by the diffused GaAs junction, the phenomenon appears to be absent in highly doped abrupt GaAs junctions.

We tentatively ascribe this difference to the following: In abrupt junctions, the zero bias space charge region extends into the N-type material of uniform carrier concentration. The measured breakdown voltage is thus

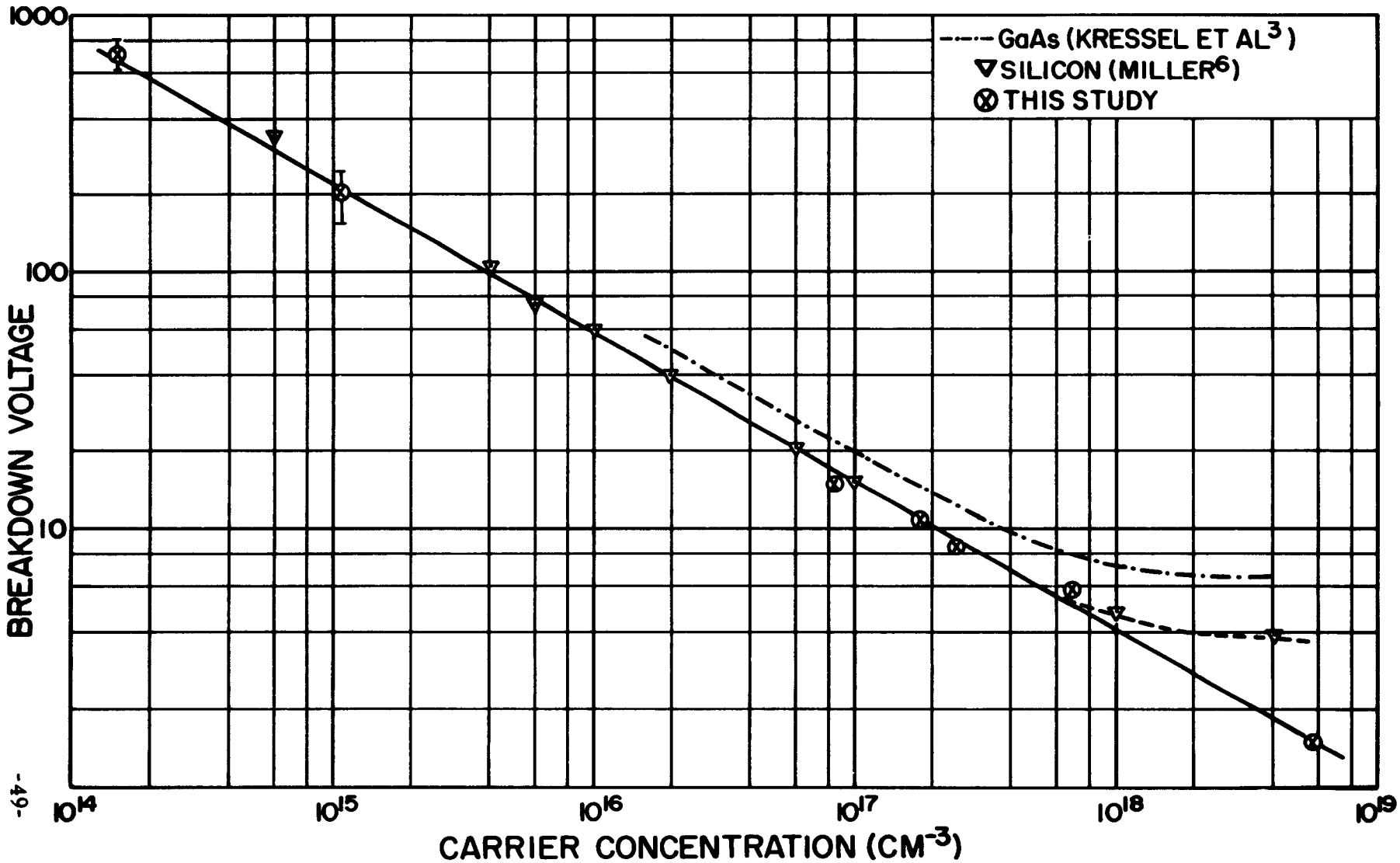


FIG. 25 The Breakdown Voltage of GaAs P^{++} on N Abrupt Junctions as a Function of Carrier Concentration

truly characteristic of the bulk. In diffuse junctions, however, the space charge may never widen into the uniform bulk region; the breakdown voltage would then be an artifact of the graded region and would not, of course, correspond to the bulk resistivity. From the data given by Kressel and others[2] no accurate estimate is possible of the width of the graded region since it is merely stated that the diffusion depth was 6 to 20 microns. The space charge width in GaAs containing 10^{18} carriers per cc is approximately 1 micron when a 7 V bias is applied. It is very likely, therefore, that at a value of $N = 10^{18}$, or greater, the data on diffused diodes no longer reflects the properties of the bulk.

(ii) Capacitance of Abrupt Junctions

The theory of the space-charge layer at a metal semiconductor interface has been developed by Schottky[4] and Mott[5]. For donors completely ionized in the bulk crystal (N-type) the capacitance may be written as:

$$C = \left(\frac{q_2 N_D K K_o}{2kT}\right)^{1/2} \frac{|e^Y - 1|}{(e^Y - Y - 1)^{1/2}} \qquad (22)$$

where

$$Y = \frac{qV}{kT}$$

when Y is strongly negative, i.e., when the bands are bent up quite strongly,

$$C = \left(\frac{q^2 N_D K K_o}{2kT}\right)^{1/2} (-1 - Y)^{1/2} \qquad (23)$$

In the limit of large negative Y this is just the Mott-Schottky approximation, and a plot of $1/C^2$ vs. Y should give a straight line, whose slope is a measure of the total donor density in the bulk. This is simply stated in the equation:

$$\frac{\partial(1/C^2)}{\partial V} = \frac{2}{n q K K_o} \qquad (24)$$

where $N_D = n$ (donors are completely ionized).

In Fig. 26 we plotted C^{-2} as a function of V for diodes of all the

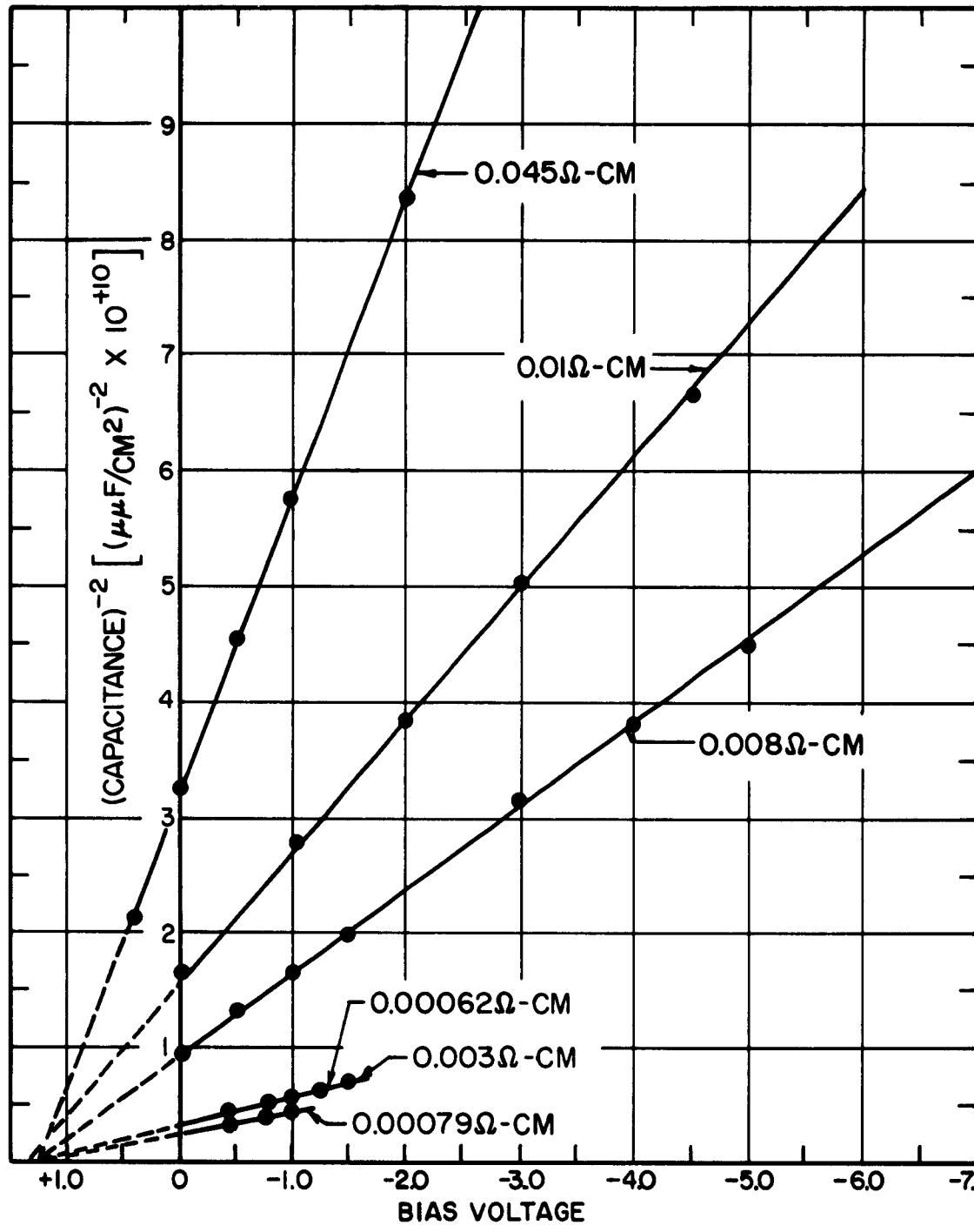


FIG. 26 Square Law Dependence of Capacitance on Voltage of GaAs P^{++} on N Abrupt Junctions

resistivities studied. As can be seen, square law behavior is followed in all cases. In Fig. 27 we have plotted $\partial\ 1/C^2/\partial\ V$ as a function of electron density (N_D). The electron density of the bulk crystals were determined by Hall mobility and conductivity measurements. The agreement with the Schottky theory is excellent in the region $N_D = 10^{15}$ to 10^{18} cm^{-3}, showing clearly that the carriers are completely ionized in the bulk. At higher donor concentrations, however, large deviations are observed. These deviations from ideal metal-semiconductor junction theory may be ascribed to the following:

(1) Errors in Experimental Measurements: Junctions prepared from low resistivity material (high donor concentration 10^{18} and above), exhibited extremely large capacitances (approximately 1,000 pf at zero bias). This is the maximum value of capacitance which can be measured on the Boonton Capacitance Bridge Model 75A58, which was used in this study. Therefore, no measurements could be made in the forward direction. Also, since the voltage breakdowns of these diodes were in the vicinity of approximately 1 volt, the capacitance-voltage function could be studied only up to 1 volt. Small errors in capacitance could, therefore, cause extremely large errors in $\partial\ 1/C^2/\partial\ V$.

(2) As a consequence of the extremely large amount of over-doping ($> 10^{18} cm^{-3}$) necessary in these diodes, the internal electron concentration of this structure was extremely complicated. This could cause extreme deviations from the Mott-Schottky relation which was derived for an uncompensated semiconductor.

(3) The space charge region in this case may spread into both the N and P type materials since both sides are relatively degenerate.

2. GaP

(a) Travelling Solvent Method (TSM)

Initial experiments were carried out to determine the appropriate method for wetting GaP with liquid Ga. It was determined that adequate wetting took place only at temperatures well above 700°C. In the first group

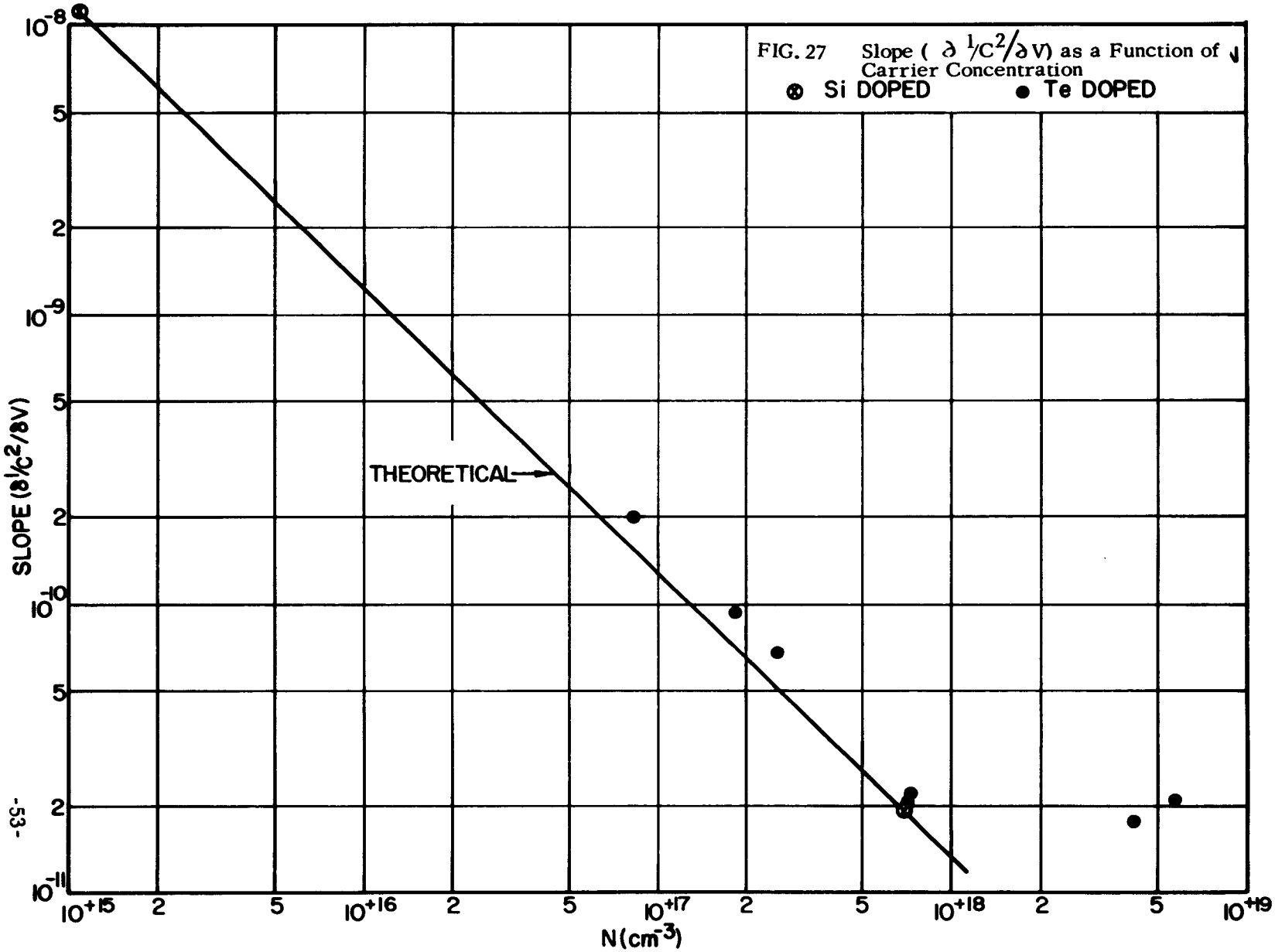


FIG. 27 Slope (∂ 1/C²/∂ V) as a Function of Carrier Concentration
⊗ Si DOPED
● Te DOPED
THEORETICAL
SLOPE (∂1/C²/∂V)
N(cm⁻³)
10⁻⁸
5
2
10⁻⁹
5
2
10⁻¹⁰
5
2
10⁻¹¹
10⁺¹⁵
2
5
10⁺¹⁶
2
5
10⁺¹⁷
2
5
10⁺¹⁸
2
5
10⁺¹⁹

of experiments, the regrowth of single crystal GaP onto GaAs from polycrystalline GaP was attempted. Since GaAs dissolves rapidly in liquid Ga at about 700°C, however, the sandwich immersion was limited to only two minutes. Metallographic examination of the sample verified that GaP had grown on the GaAs substrate. Also, X-ray analysis confirmed the single crystal nature of the deposit. Movement, however, was limited to only 1 or 2 mils, the regrown layer being a mixture of GaAs and GaP. Since GaP has recently been reported[6] to be more soluble in Sn and In than Ga, zone movement experiments were carried out using these solvents. The use of Sn met with only limited success. In order to obtain adequate wetting of the source and substrate crystal, it was necessary to employ zones of at least 4 to 5 mils in thickness.

In all cases, Sn dissolved the GaAs violently, thereby impeding zone movement. When the growth of GaP on GaP was attempted using Sn zones, zone movement again did not occur. Large amounts of precipitated GaP crystals were found in the Sn solvent zone. In this case, the liquid diffusion of GaP in the thick Sn zone may have been slower than the rate of solution of the GaP.

Using the existing GaAs system, a large amount of phosphorus vaporization was observed. To eliminate this, the experimental set-up shown in Fig. 28 was employed. The phosphorus placed at the cold end (400°C) of the sealed quartz furnace tube maintained an equilibrium pressure of phosphorus over the GaP structure at 950°C. Very little vaporization took place over a period of three hours. Using this system, however, only negligible amounts of regrowth were observed. This difficulty was basically involved with the attainment of a sufficient gradient for zone movement. It was found that when using the 100 mil sandwich of GaP-Ga-GaP, a temperature gradient of approximately 220°C was necessary before significant zone movement occurred. To obtain this temperature gradient, and also to prevent an extensive loss of phosphorus from the system, the set-up shown in Fig. 29 was employed. Gradients in the vicinity of 3°C per mil were obtained in this system without significant GaP volatilization. A photomicrograph of one of the junctions prepared in this system is shown in Fig. 30. It may be seen that far above the junction region polycrystalline GaP was beginning to form. As a consequence of the high impurity concentration of the P-layer, light could only be

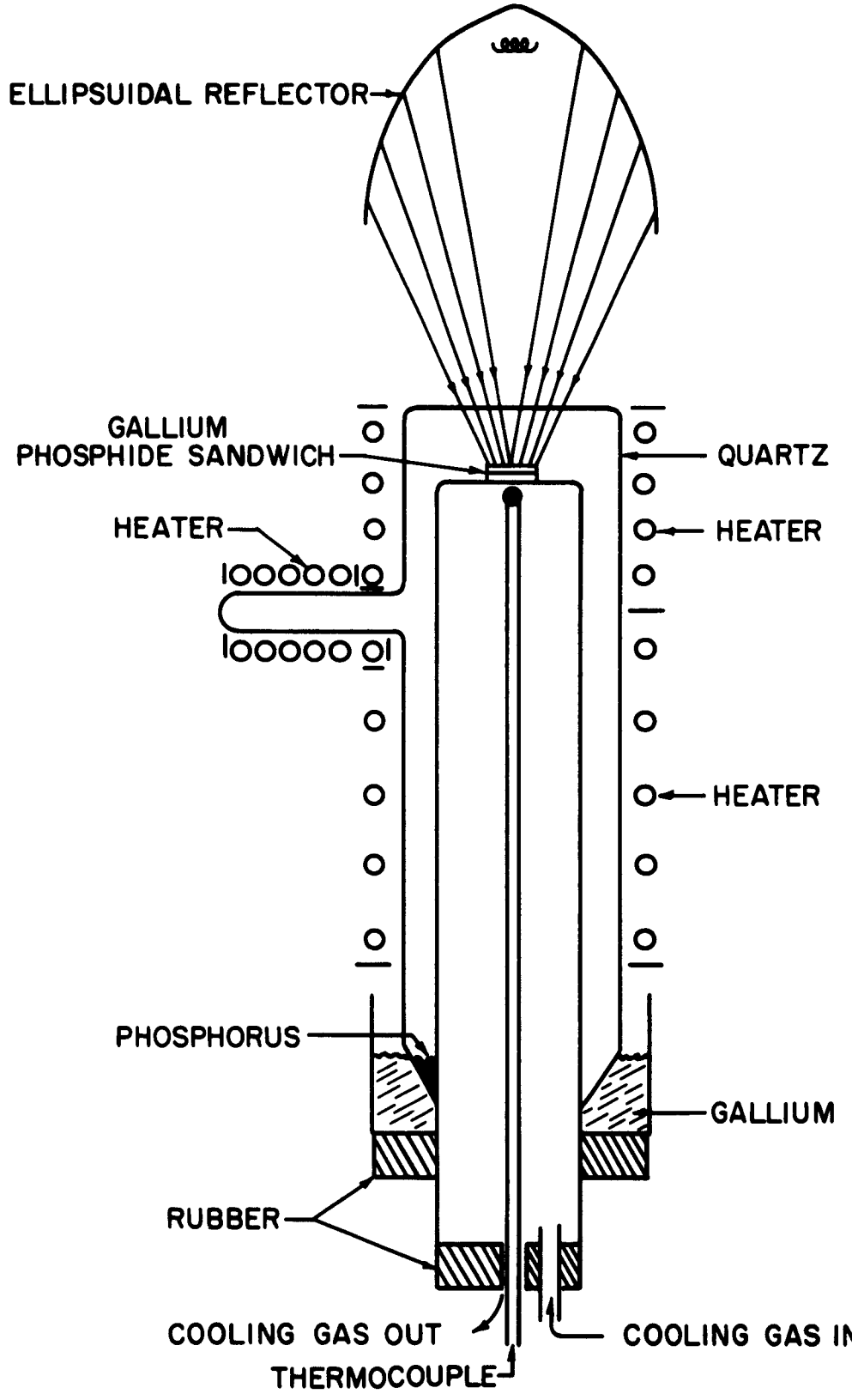


FIG. 28 **APPARATUS FOR GaP MOVEMENTS**

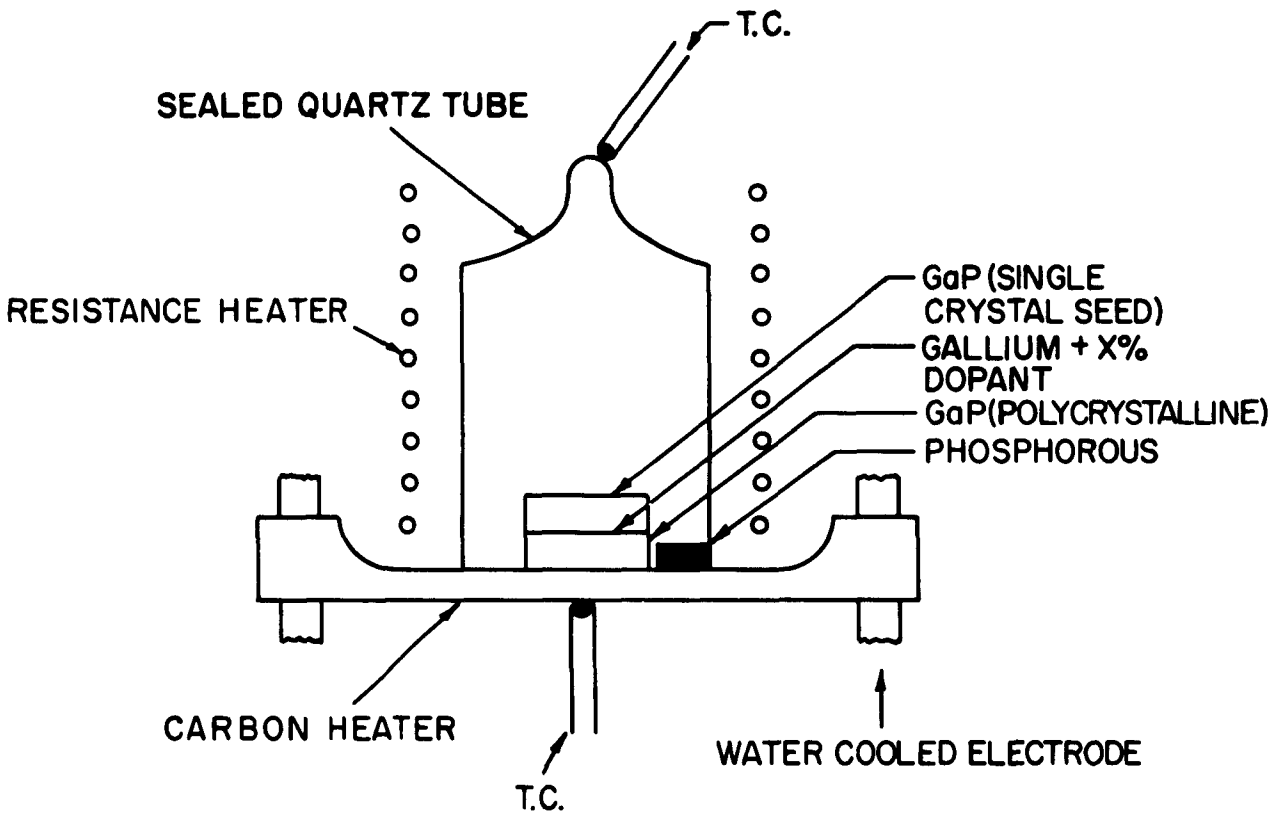


FIG. 29 GaP ZONE MOVEMENT SET-UP

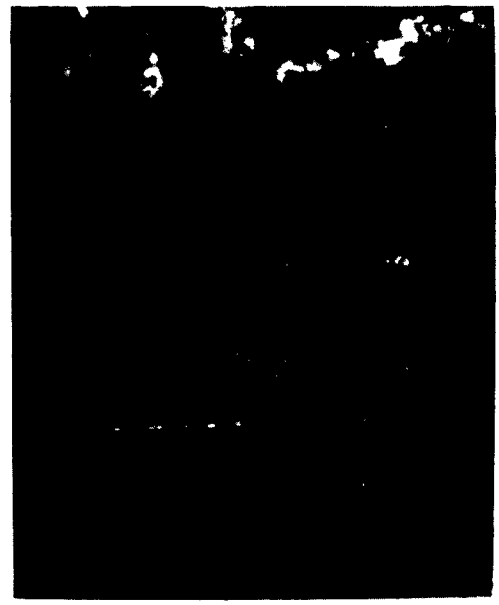


FIG. 30 GaP Junction Prepared by TSM (unetched) 100 X

transmitted through the N-GaP. This was an excellent check on a junction character of the prepared structure. Thus far, however, erratic electrical results have been obtained for junctions prepared from single crystal material (single crystals were prepared by Harshaw Corporation by precipitation from a gallium melt). Large numbers of cracks and porosity were observed in the crystals we received. These defects contributed to the fracture of the zone by allowing gallium to seep through and across the junctions. The straight line at the lower edge of the gallium phosphide regrown diode (Fig. 30) is a typical example of the crack structures found in these crystals.

As a consequence of the difficulties encountered with the single crystal material, diode fabrication was attempted using polycrystalline substrates. A higher degree of success was encountered using this 100% dense material. In all cases the orientation and structure of the substrate crystal was perpetuated by the regrown crystal. Fig. 31 is the TSM composite using a polycrystalline seed. As can be seen, the grain boundary of the substrate crystal was carried into the regrown crystal. The etch pits demonstrate that the substrate crystal orientation was perpetuated by the regrown crystal (crystal etched in methyl chloride etch for 20 minutes). The Ge-doped regrown GaP crystal was found to be high conductivity P-type by hot probe analysis. Initial electrical measurements on large area (40 mil diam.) GaP chips gave inconclusive results. It was necessary to etch down the chips to approximately 5 mils in diam. in order to remove random grain boundaries and other defects. Ohmic contacts were made to the N and P sides of the junction by using Ag-Te and commercial silver solder wires respectively.

(b) Electrical Evaluation of P^{++} on N Junctions

Typical forward and reverse characteristics of gallium phosphide junctions are shown in Figs. 32 and 33 respectively. A straight line is obtained in the current range 10^{-4} to 10^{-7}A for forward characteristics (at 20°C) with a slope of E/η kT, where η = 3; e = electron charge; k = Boltzman constant; T = absolute temperature. The value of η is found to lie between 3 and 4 for all the junctions studied and may be ascribed to

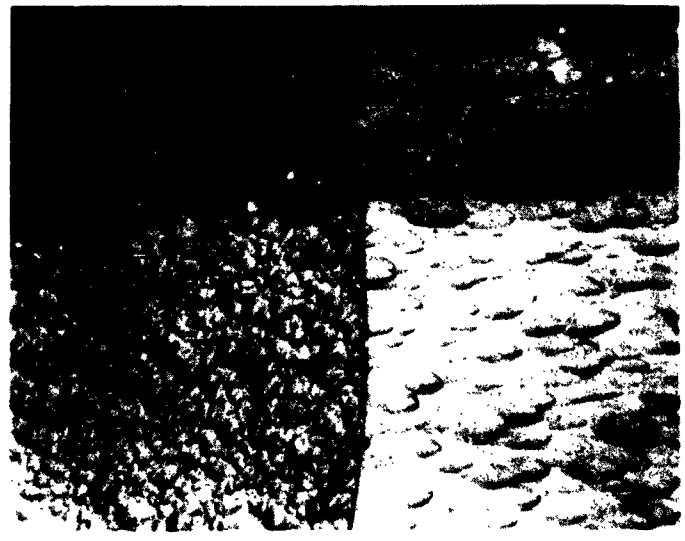


FIG. 31 GaP Junction Grown by Using a Polycrystalline Seed (etched in Aqua-Regia) 50X

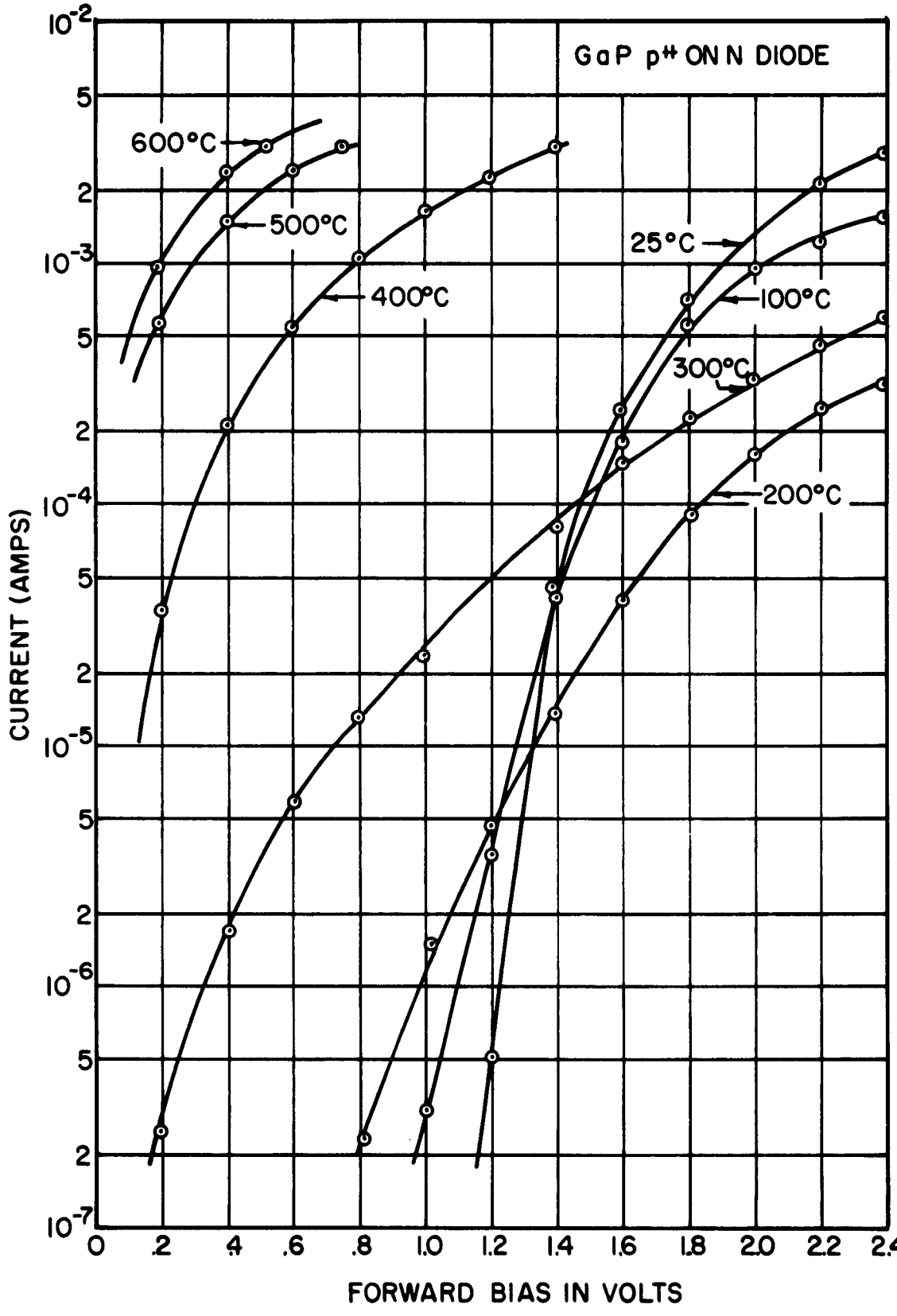


FIG. 32 Forward Characteristics of GaP TSM P^{++} on N Junctions as a Function of Temperature

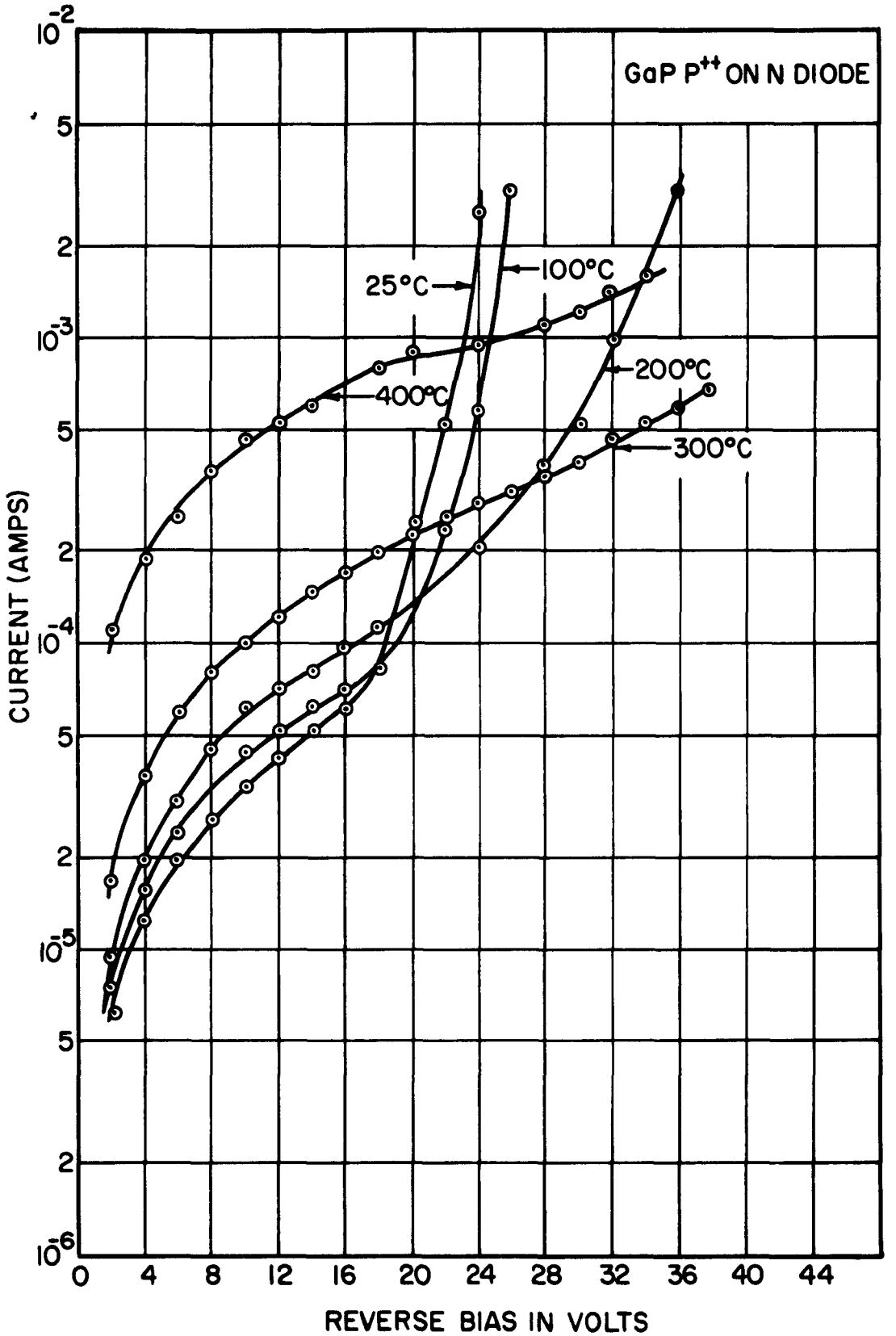


FIG. 33 Reverse I-V Characteristics of GaP TSM P^{++} on N Junctions as a Function of Temperature

non-linear carrier recombination. All diodes studied had relatively soft reverses as can be seen from Fig. 33. Currents as small as 20μA were obtained up to reverse biases of 30 volts for some diodes. However, again sharp breakdown was not observed. The I-V characteristic as a function of temperature indicated that the breakdown voltage (at 20μA) decreased with increasing temperature as would be expected.

Rectification ratios of 10^2 were obtained at 400°C. Rectification was nil at temperatures above 500°C. The absence of a sharp breakdown made the determination of the breakdown voltage as a function of resistivity inconclusive.

C. EPITAXIAL GROWTH OF GaAs AND GaP

1. GaAs

Many techniques have been presented in the literature for the growth of epitaxial GaAs. They can, in general, be divided into two main categories, namely, closed tube and open tube techniques. Since the former technique involves a minimum of equipment, it was tried initially.

Closed Tube Epitaxy: This technique involves the transport of gallium and arsenic through the vapor phase by chemical reaction with a metal halide to form a volatile species. At a lower temperature, these species dissociate to form GaAs which grows on a single crystal seed of GaAs or another appropriate substrate. Fig. 34 is a sketch of the apparatus used. It consists essentially of a two-zone furnace in which a sealed evacuated quartz tube is placed. The tube contains the GaAs source material at the hotter end and a GaAs seed crystal at the cooler end. A metal halide is also enclosed. In a typical experiment, the seed crystal was of the (111) orientation, the source material was 2 grams of high resistivity GaAs, the carrier was 0.020 grams $SnCl_2$, and the deposition temperature was 500 to 675°C. Fig. 35 is a photomicrograph of the deposit on the A or gallium face, which was exposed to the vapor. Characteristic pyramidal growth was observed on the (111) B-face. The influence of polarity of the (111) surface has also been noted by Williams and Ruehrwein[7]. Although very tenacious single crystal epitaxial layers were grown by this approach, extremely long and tedious experimental times were necessary to prepare for a single run. For this

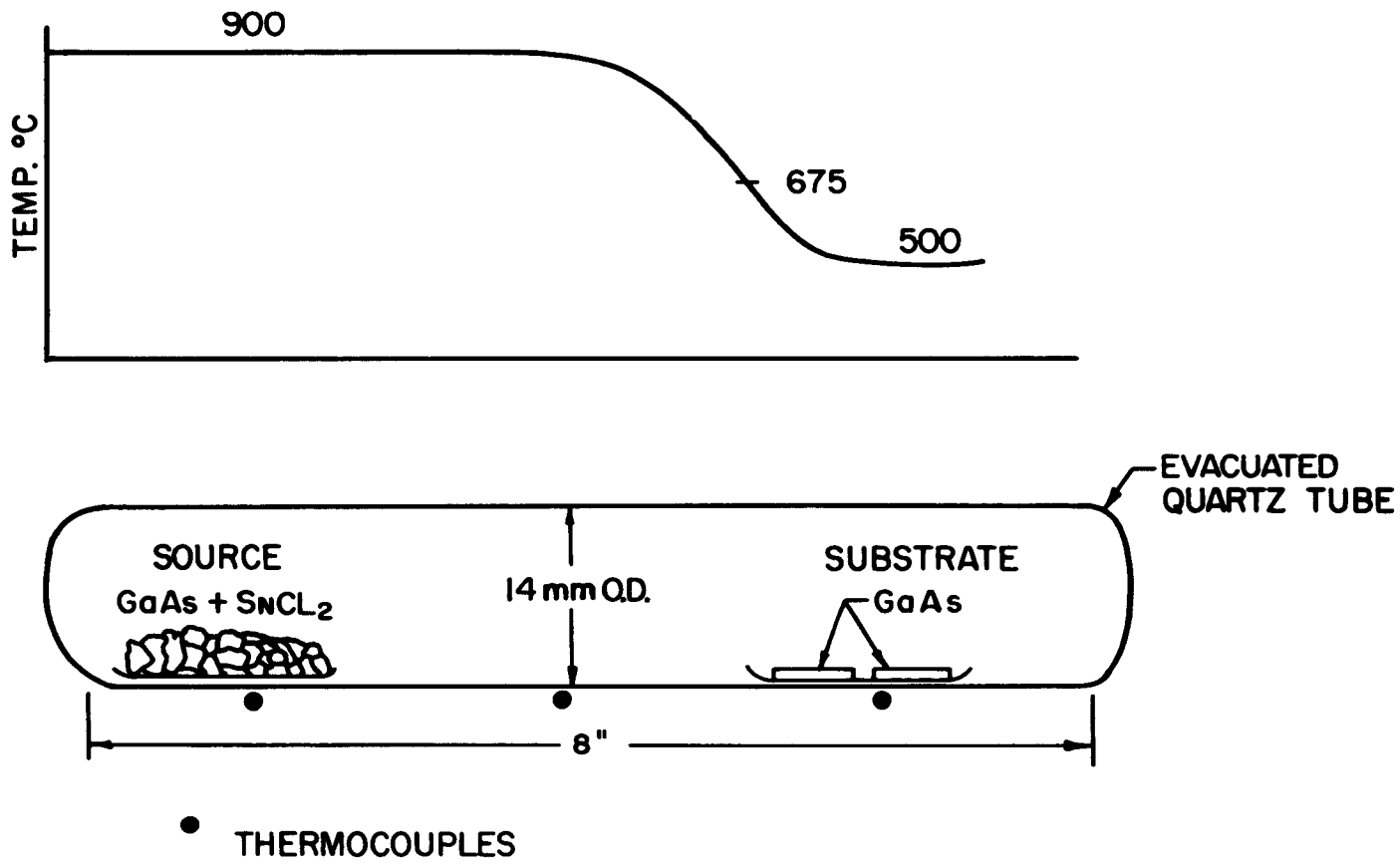


FIG. 34 CLOSED TUBE EPITAXIAL DEPOSITION SYSTEM

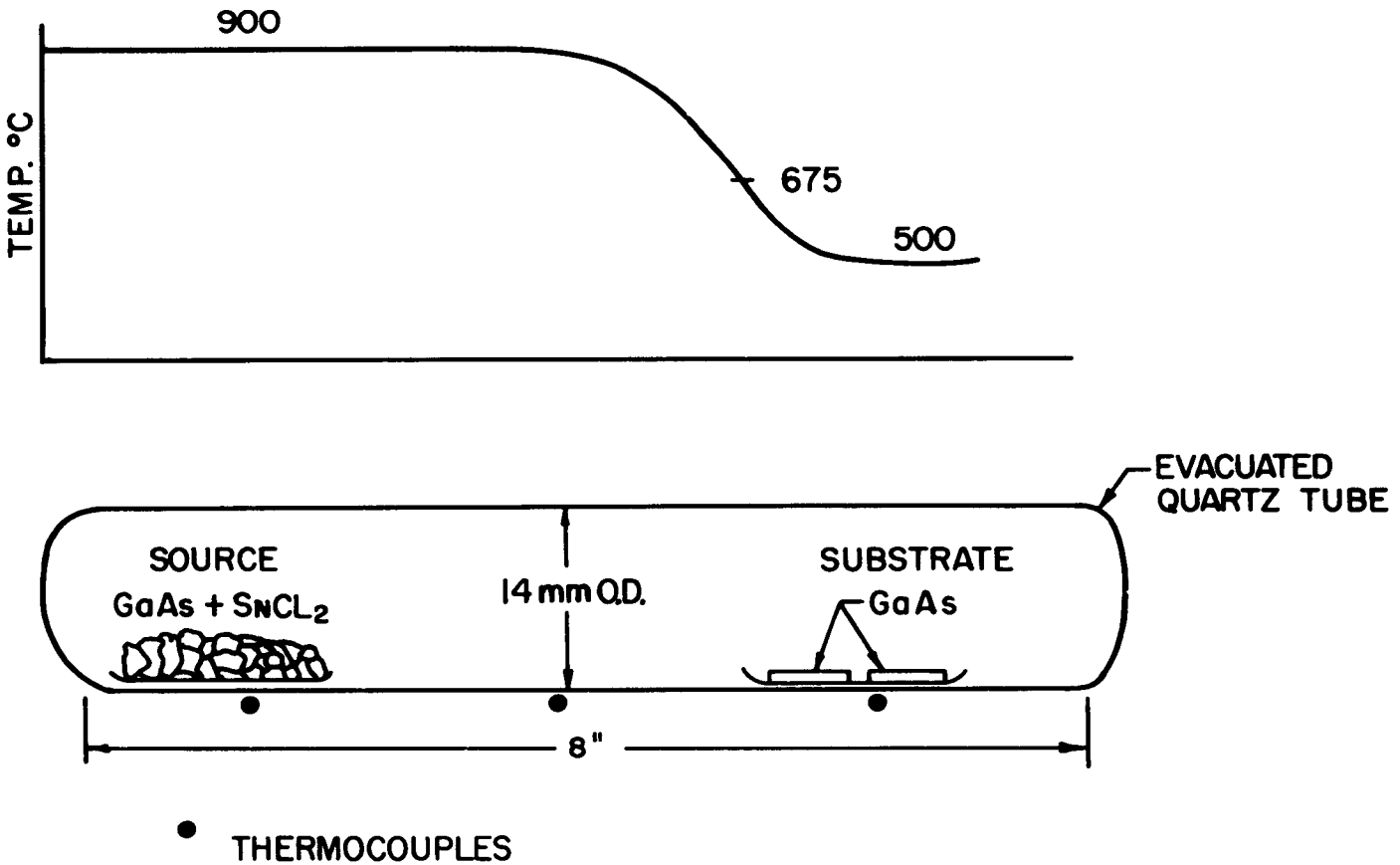


FIG. 34 CLOSED TUBE EPITAXIAL DEPOSITION SYSTEM

FIG. 35 Epitaxial Growth of GaAs on A-$(111)_{Ga}$ Face of GaAs (15X)

reason, the technique was discontinued in favor of the open tube approach which is inherently much more easily accomplished when the equipment is in operation.

(a) Epitaxial Growth Using HCl Carrier Gas Technique

An investigation of the epitaxial growth of GaAs by open tube vapor transport technique has been carried out. The experimental variables studied were temperature, temperature gradient, crystal orientation, surface preparation, and gas flow rate. The use of HCl as a possible transport media for the process of epitaxial deposition of GaAs has been advanced by Newman and Goldsmith[8] and Williams and Ruehrwein[7]. The reaction occurring between the source GaAs and the HCl is given by the equation:

$$GaAs + HCl \rightleftharpoons GaCl + 1/4\ As_4 + 1/2\ H_2 \qquad (25)$$

The following equation describes the reaction which occurs in the deposition region:

$$3\ GaCl + 1/2\ As_4 \rightleftharpoons 2\ GaAs + GaCl_3 \qquad (26)$$

The deposition reaction was postulated since large quantities of $GaCl_3$ and free As are found at the exit sections of the reaction tube. Transfer mechanisms are oviously different for the two elements involved. The gallium is seen to form lower halides which disproportionate on the substrate surface, whereas the arsenic evaporates and is transported by the carrier gas to the seed crystal.

(i) Experimental Results

The furnace set-up used is shown in Fig. 36. The HCl was purified by passing it through a cold trap of acetone and dry ice. To remove the possibility of metallic contamination, all the valves for transporting the HCl were made of stainless steel or monel. The hydrogen used was first passed through a deoxo unit (platinized palladium pellets) to remove oxygen and then was passed into a drying tower to remove any H_2O vapor. Quartz was the only material, other than the seed and source materials, which was used in the hot zones of the reaction chamber. During the initial investigation

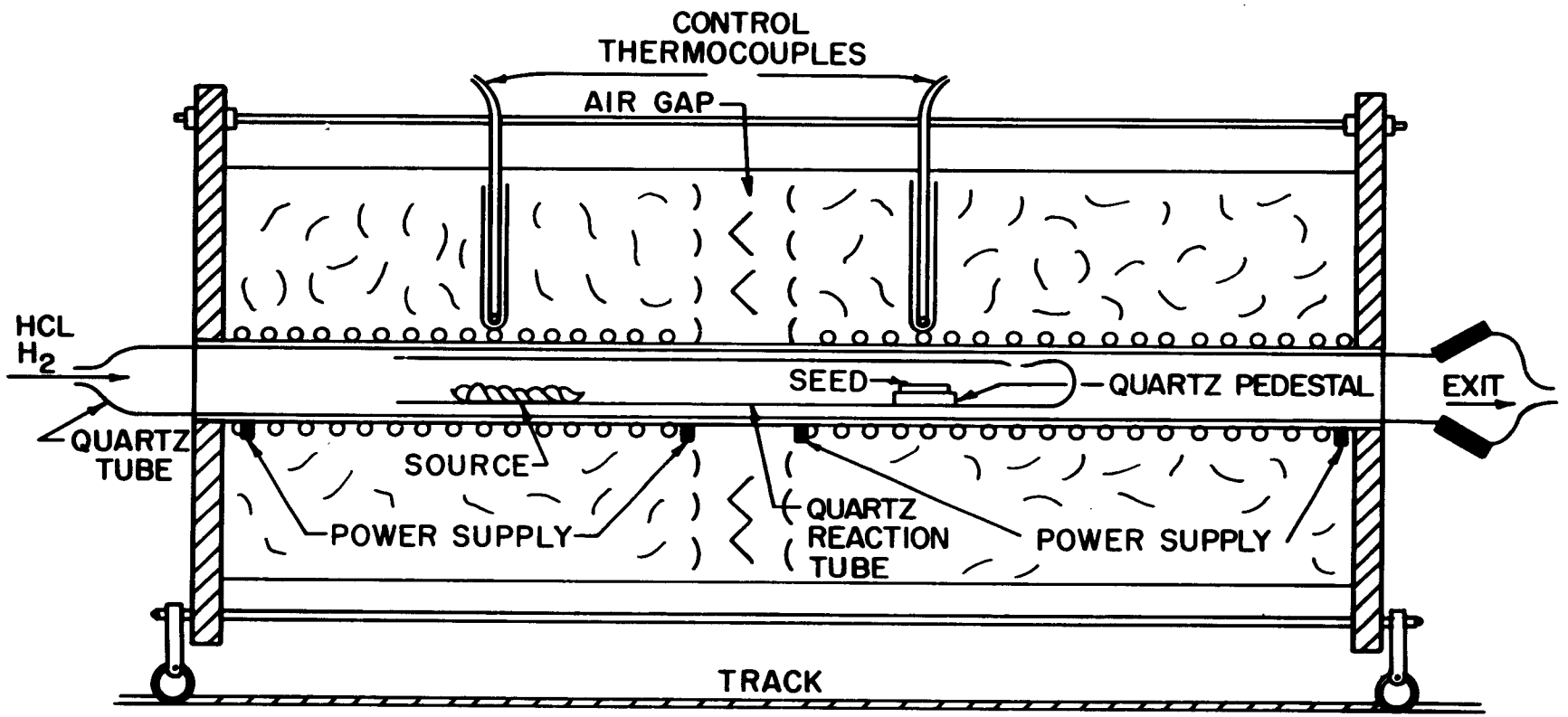


FIG. 36 TWO ZONE EPITAXIAL FURNACE

of the process variables, a large multiple tap resistance furnace was employed. This facilitated the variation of the source and seed temperautres. The experimental procedure was as follows:

The source and the seed materials were etched in a modified CP4, and the orientation of the seed noted. Seed crystals were then carefully polished to a mirror-like finish. The source and seed materials were then placed into a quartz reaction tube (at the desired position) and the system was purged with helium. Hydrogen was then passed through the system for half an hour. With hydrogen still flowing through the system the furnace was moved on its track so as to place the source and seed crystals at the proper temperature. When the desired source and seed temperatures were obtained, the desired mixture of HCl and H_2 was passed into the reaction chamber. After the reaction period, the furnace was quickly moved away from the source and seed materials, and HCl flow was stopped. Slight amounts of powdered material were deposited on the surface of the seed films; however, they could be removed by merely washing ultrasonically in acetone. The results of these experiments to determine the optimum process variables will be discussed using the data of Table VII in conjunction with photomicrographs of the epitaxial deposits.

The source temperature, substrate temperature, and the temperature drop between the seed and the substrate, were found to be extremely critical to the epitaxial growth process. When the source temperature was higher than 850°C, the rate of material transfer was extremely fast, thereby making the gas flow much too critical. To eliminate this problem, the source temperature was maintained at 850°C in the majority of experiments. The effect of seed crystal temperature on the nature of the deposit was studied. In runs 5 and 6 (Table VII) the seed temperature was 800°C and 792°C, respectively. Although there was some etching of the seed in both cases, there was also some deposit on samples 5 and 6. Fig. 37 shows large growth figures on the extreme portion of the crystal. These etch figures are similar to the growth facets apparent on the surface of a (111) GaAs oriented crystal grown from solution. Structures of this type are not normally obtained by "aqueous" etching techniques. The downstream portion of the crystal may be seen in Fig. 38. Fairly flat smooth epitaxial deposition has occurred on this portion of the crystal. The surface texture may be described

TABLE VII

Results of Epitaxial Growth Experiments (GaAs)

Run	Source Wt. Loss	Temperature °C Source		Seed	HCl Flow cc/min	H_2 Flow cc/min	Time Min.	Face	Wt. Gain	Speed
1	.8444	915	1	725	10	80	60	-	1	.0070
			2	600					2	.0028
			3	550						
			4	475						
2	none left	870	1	770	10	80	77	B	none left	
			2	725				B		
3	.3258	800	1)	650	4.0	40	35	A	1	.0006
			2)					B	2	.0010
			3	575				B	3	.0012
4	.3237	856	1	788	4.0	40	70	B	1	.0008
			2	741				B	2	.0189
			3	687				A	3	.0172
5	.8736	850	1	800	4.0	40	75	B	Lost weight	
			2	800				B	1	.00349
									2	.00269
6	1.4011	850	1	792	5.0	40	85	B	Lost weight	
			2	792				B	1	.04099
									2	.0497
7	1.1633	850	1	765	3.0	35	75	B	1	.0113
			2	745				B	2	.0073
8	.5609	850	1	765	2.0	30	60	B	1	.0073
			2	745				B	2	.0055
9				Poor run						
10	.9269	850	1	765	4.0	40		B	1	.0212
			2	745				B	2	.0164

TABLE VII Results of Epitaxial Growth Experiments (GaAs)

Run	Source Wt. Loss	Temperature °C Source	Seed	HCL Flow cc/Min.	H_2 Flow cc/Min.	Time Min.	Face	Seed Weight Gain (grams)
11.	0.1619	870	763	3	30	110	A	0.0003
							B	0.0002
12.	0.5316	870	735	3-3.5	35	75	A	0.0017
			763					0.0032
13.		870	735	3	30	70	B	0.0052
							A	0.0048
14.	.489	870	735	3	30	70	A	0.0041
							B	0.0025
15.	---	870	735	3	25	62	A	---
16.	.5014	870	735	3	25	60	A	0.0084
17.	0.5481	870	735	3	25	60	A	0.0048
18.	0.4005	870	735	3	25	60	A	0.0137
19.	0.5450	870	735	3	25	60	A	0.0136
20.	0.4791	870	735	3	25	60	A	0.0043 Area= 0.503cm^2
21.	0.5344	870	735	3	25	60	A	0.0047 Area= 0.503cm^2
							B	0.0027 Area= 0.25cm^2
22.	0.5770	870	735	3	25	60	A	0.0062 Area= 0.64cm^2
							B	0.0068 Area= 0.64cm^2
23.	0.1368	870	735	3	25	30	A	0.0037 Area= 0.6cm^2
24.	0.8903	870	735	3	25	120	A	0.0170 Area= 0.6cm^2

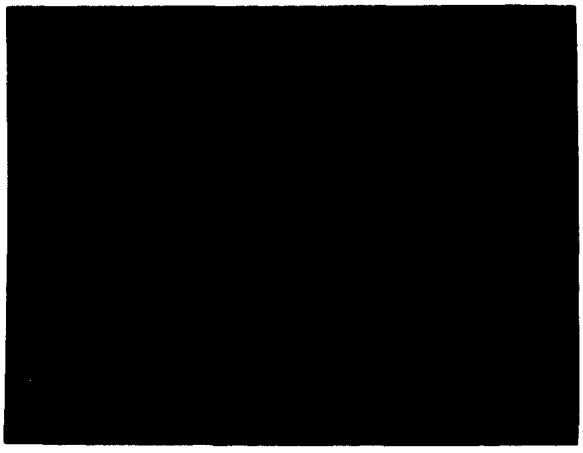


FIG. 37 Large Etch Figures of Upstream Portion of Crystal IV-2 (unetched) 300X

FIG. 38 Micro-Orange Peel Pattern of Epitaxial Growth on Downstream Portion of Crystal IV-2 (unetched) 300X

by the term "micro-orange peel pattern". This type of texture is one of the smoothest obtainable. This type of surface texture has been correlated to the dislocation density of the deposit (in silicon by Glang and Wajda[9]), who have approximated the dislocation density for this type of texture to be below 10^5 cm^{-2}. The variation in perfection of the deposit may be explained by the reasonably large temperature gradient in the furnace which caused a 50^oC temperature gradient across the seed crystal. In order to obtain large area extremely smooth epitaxial films, the two-zone furnace shown in Fig. 36 was employed. The results obtained will be described in a later section.

The effect of temperature difference between the seed and source materials is brought out clearly by deposits on samples III-3 and IV-2, which are shown in Figs. 39 and 40, respectively. With the source material at 800^oC and the seed at 575^oC (Fig. 39), large numbers of small crystallites nucleated on the crystal surface. A more dramatic occurrence of the previous deposition mechanism may be seen in Fig. 40. The complete polycrystalline formation occurred due to the relatively high source temperature and the extremely high temperature difference; these increased the rate of deposition between the source and the seed crystal. Fig. 41 shows the tendency to oriented overgrowth in run II when the temperature difference between the seed source and seed was approximately 68^oC. The temperature situation found most suitable for epitaxial growth was the source at 850^oC and the substrate at 765^oC. The epitaxial films obtained using these temperatures will be explained in the next section.

Flow Rate: The interaction of flow rate and temperature effects in this system has been studied. Using a flow rate of HCl = 3.0 cc/min. and H_2 = 35 cc/min., with the optimum temperature gradient of 85^oC, the chevroned pattern-type epitaxial film shown in Fig. 42. was formed (VII-I). This type of surface was characteristic of a dislocation density greater than $10^5/cm^2$. By increasing the temperature gradient by 20^oC, the pyramidal growth facets typical of growth on a (111) plane have started to form along the chevron markings. The voltage breakdown of these two epitaxial layers measured by the point contact technique were 10 and 25 volts, respectively. These correspond to resistivities of 0.01 and 0.08 Ω-cm, respectively. The thickness of the epitaxial layers as calculated from the measured weight gain and angle lap-staining techniques are approximately

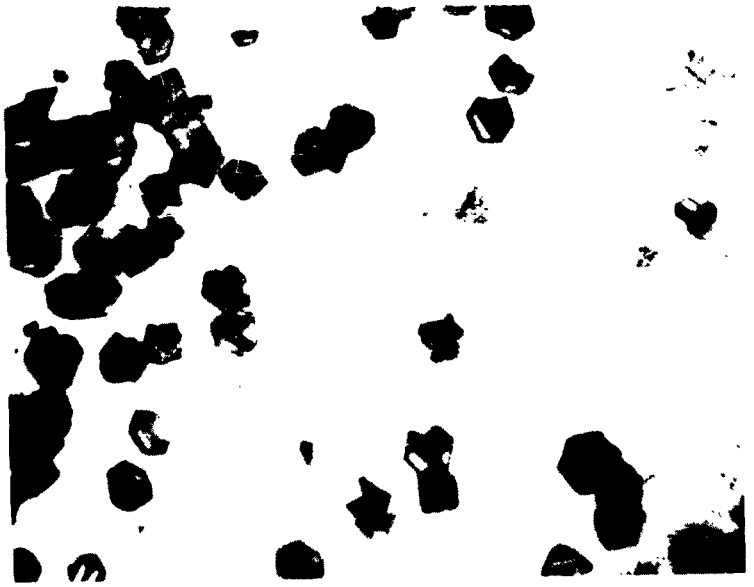


FIG. 39 Nucleation of Small Crystallites on the Surface of Crystal III-3 (unetched) 300X

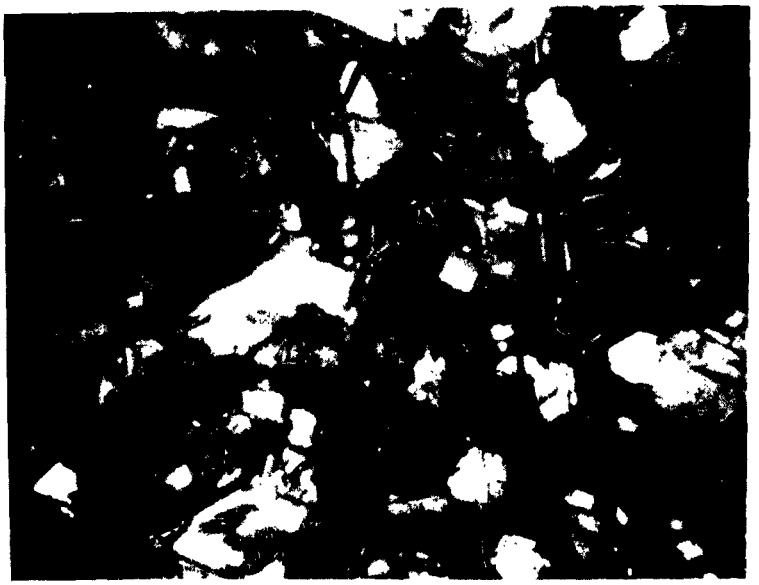


FIG. 40 Polycrystalline Deposit on Crystal IV-2 Showing Effects of Thermal Temperature Differential (unetched) 60X

FIG. 41 Tendency Toward Oriented Overgrowth on Crystal IV-1 (unetched) 300X

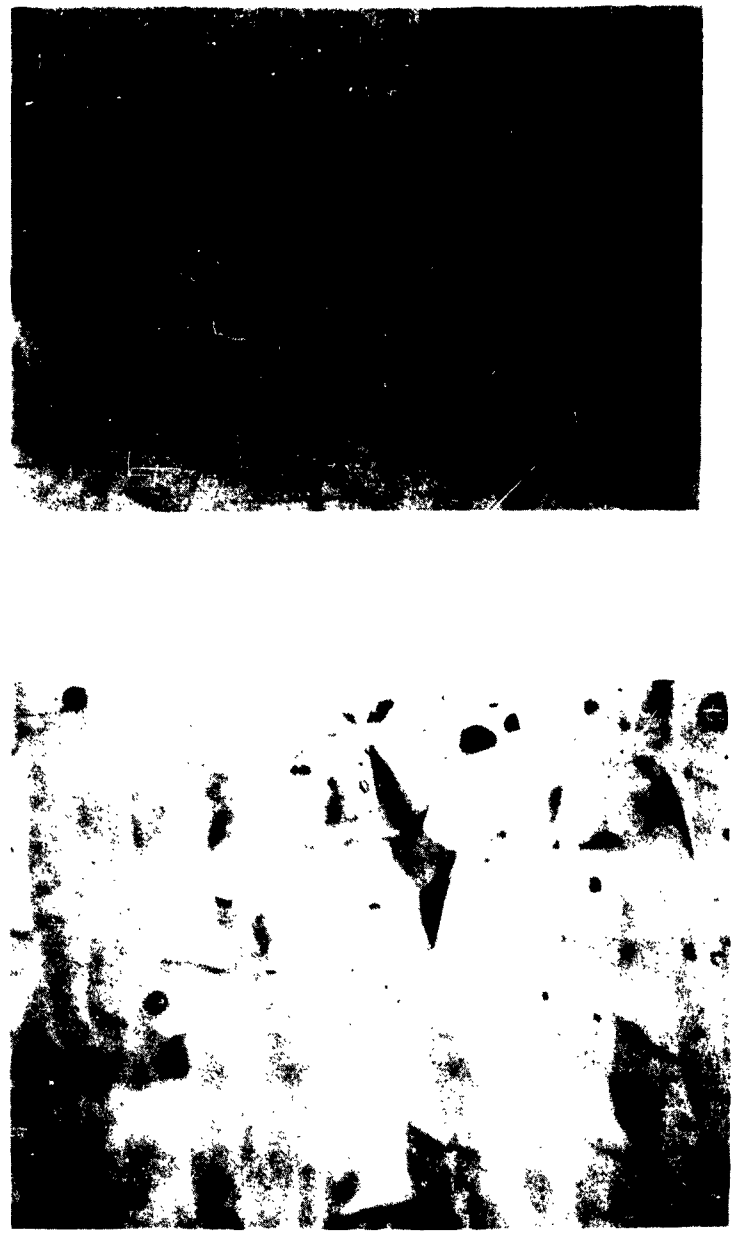


FIG. 42 Chevroned Pattern of Epitaxial Deposit on Crystal VII-1 (unetched) 300X

10 microns for sampleVII-I and 8 microns for sample VII-2. Using a lower flow rate, HCl = 2.0 cc/min, and H_2 = 30 cc/min., the epitaxial film (IX-I), Fig. 43, was formed. Facetted growth was produced because of the slow deposition rate.

Surface Preparation:. It is well known that one of the major factors in the preparation of smooth highly perfect epitaxial films is the condition of the substrate surface. Initially a great deal of trouble was encountered in the preparation of highly polished gallium arsenide surfaces. Mirror-like finishes could be obtained by mechanical polishing. However, it became obvious that the strained surface layers did not lend themselves readily to smooth epitaxial deposits. When GaAs was etched, with the polish etches normally used for Ge and Si (HF and HNO_3 of various proportions and concentrations) poor surfaces were obtained in all cases. Of all the common chemical etchants, aqua regia produced the best surfaces. However, preferential etching did occur. The surface preparation procedure finally decided upon involves the use of the chemical polish etchant first described by Fuller and Allison[10]. The etching consisted basically of an organic liquid in which chlorine or bromine is dissolved. For GaAs the best results obtained in this laboratory were accomplished by using an etch prepared by bubbling chlorine gas slowly through methyl alcohol, with the specimen completely immersed. A reproducible etching rate of approximately 0.5 mils/min. at 25°C was obtained with the solution completely saturated with gas (a yellow solution indicated saturation). It was found that the most highly polished surfaces were obtained when the specimen was placed within 1/4 inch from the gas entry nozzle. The solution color was darkest at the gas nozzle and decreased in intensity as the surface was approached. Correspondingly, the rate of etching was found to decrease considerably as the sample was moved successively farther from the nozzle entry point. A negligible amount of etching occurred when the sample was approximately 1 inch (vertical direction) from the entry nozzle. Utilizing this surface preparation technique in conjunction with the two-zone furnace shown in Fig. 36 and the experimental parameters determined previously (source temperature 870°C, seed temperature 735°C, HCl flow 3 cc/min., H_2 flow 25 to 30 cc/min.), very smooth and highly perfect epitaxial layers of GaAs have been deposited upon GaAs

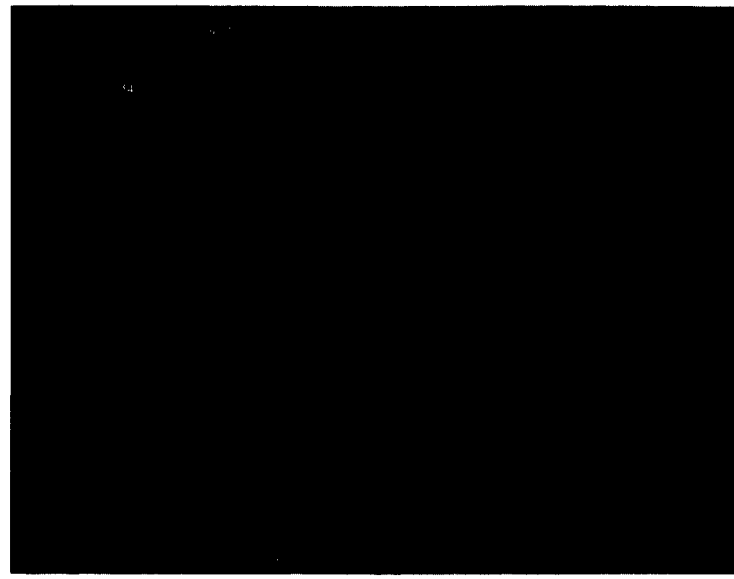


FIG. 43 Facetted Growth on Epitaxial Deposit on Crystal IX-1 (unetched) 300X

seed crystals (see Fig. 44). The results of 14 runs performed using this finally adopted technique are given in Table VII (#11 and #24). As indicated, many of these epitaxial deposits have been used as the active layer of the TLI point contact varactor diodes. The electrical results obtained from these diodes will be reported in a later section. As can be seen from the appropriate data, the rate of etching of the source material and the rate of crystal growth are extremely reproducible from run to run. The average rate of crystal growth under the existing conditions was found to be 10 microns per hour. Two additional runs were made in order to ascertain whether there was a necessary incubation period for the deposition process. As can be seen from the data in Table II, the rate of growth was constant with time. It was, therefore, possible to prepare epitaxial layers of desired thicknesses from 1 to 100 microns with accuracies of $\pm$10%. The rate of film growth was found to be independent of (111) polarity as was found by Williams and Ruehrwein[7]. The perfection of the film was also found to be independent of crystal polarity. However, the defects formed on the surface were particular to that specific surface face. Thickness variations of less than 10% were observed over most of the substrate area.

(ii) Electrical Evaluation of Epitaxial Deposits

Point contact varactor diodes were prepared in order to study the electrical properties of the deposited GaAs layers. The properties of the prepared diodes are given in Table VIII. They compared favorably with those obtained using the epitaxial GaAs obtained by the Monsanto Chemical Corporation. The ϕ values of the point contact diodes tested were approximately 1 to 1.25. the value of η* varied from approximately 1 to 3.6. The effect of source material resistivity upon the epitaxial deposit was studied in runs 13 - 20. In runs 13 through 16, a source material resistivity of approximately 0.01 Ω-cm was used. The resulting epitaxial film possessed a voltage breakdown of approximately 1 to 3 volts. This indicated a layer

---

* η is related to the I vs. V characteristic by the equation:

$$I = I_0 (eV/\eta kT - 1)$$

FIG. 44 Smooth GaAs Epitaxial Film. Films 1 cm^2 have been grown with as few as one of the wrinkled defects shown (unetched) 300X

TABLE VIII

Electrical Properties of GaAs Varactor Diodes*

Exp. #	V_b(volts)	V_f(volts @3ma)	C_o ≠ pfd	VSWR(db) (-0.4V)	fc at -2V KMC		N_f 2 log I/aV
16.	7.2	1.0	0.675	14.7	180	-1.07	1.36
19.	5.2	1.08	0.818	10.2	120		
20.	6.0	1.0	0.526	13.4	163	-1.03	2.05
30B.	4.0	1.25	0.540		108	-1.25	3.6

* Substrate 0.0006 - 0.0008 Ω-cm (V_b = 1-2 volts)

≠ Measurement in Cartridge Package at 10 KMC

C_o includes package capacitance

resistivity of 0.006 - 0.001 Ω-cm, which was within the resistivity region of the initial substrate material. .Using a source material which had a specific resistivity of 0.1 Ω-cm (silicon doped), the epitaxial layers possessed voltage breakdowns from 6 to 10 volts. Using the data obtained for P^{++} on N GaAs diodes, this value of breakdown corresponds to a resistivity of approximately 0.003 to 0.01 Ω-cm. Using 1 Ω-cm source material, breakdowns in the vicinity of 20 to 25 volts were obtained. This corresponds to a resistivity of approximately 0.1 Ω-cm. It is, therefore, obvious that in the process of transport and deposition the gaseous species pick up impurity from the reaction tube. It is most probable that silicon is leached from the quartz tubes at high temperatures and is deposited on the substrate crystal to increase the conductivity of the deposit.

In one run, GaAs platelets were deposited upon gold-plated Kovar pins using the same procedure as was reported for the epitaxial deposition process. The advantages of this process are (1) it eliminates completely the necessity for making an alloy contact to the GaAs since at the temperature of deposition Au and GaAs form an extremely excellent ohmic contact, and (2) it eliminates the necessity for the GaAs substrate, therefore decreasing the R_s of the device. Very good varactor diodes were obtained using this technique, (f_c = 100 KMC at -2V). There is a possibility that the contacts prepared by the direct fusion of gold and gallium arsenide were resistive as shown by the high value of η = 3.6.

2. GaP

(a) Epitaxial Growth Using HCl Carrier Gas Technique

The system used in this study was similar to that described by Ing and Minden[11]. This is approximately the same transport system as described for the gallium arsenide study. However, the synthesis of GaP was accomplished directly in the reaction chamber. In this study, HCl gas is passed in a H_2 stream over heated phosphorus and over gallium (at higher temperature). An epitaxial deposit is obtained on the seed which is held at a lower temperature than the gallium. The controlling equilibrium chemical

equations are as follows:

At Source:

$$Ga + X\ HCl \rightleftharpoons GaCl_X + 1/2\ X\ H_2 \qquad (27)$$

At Seed:

$$3\ GaCl_X \rightleftharpoons (3-X)\ Ga + X\ GaCl_3 \qquad (28)$$

These equations are similar to those previously specified for the GaAs system. 35 runs were accomplished in order to determine the most optimum parameters for epitaxial growth of GaP.

(i) Experimental Results

During the initial experiments, the source gallium was placed at 870°C and the seed GaAs at 765°C. Source phosphorus in all cases was kept at a temperature of approximately 300°C. See Table IX for results. The diagram of the experimental set-up is shown in Fig. 45. Again, a two-zone furnace was used to accomplish the epitaxial deposition process. Using a source gallium temperature of 870°C and a seed GaAs temperature of approximately 735 to 765°C, fuzzy yellow deposits of GaP were found on the seed crystal. These deposits could be easily removed from the crystals. Using this temperature distribution and a flow rate of HCl of 3 to 8 cc/min. and H_2 of 25 to 45 cc/min., etching of the seed crystal was observed. In order to increase the rate of formationof GaP, the source Ga was placed at a temperature of 970°C, the seed crystal remaining at 700 to 750°C. Yellow deposits were again observed on the substrate crystal. The formation of red crystalline GaP, however, was now observed at the hotter sections of the furnace (approximately 800 to 850°C). When the seed crystal was placed in this zone, the source material remaining at 950°C, massive GaP deposits were found on the substrate crystal. In some cases, GaP layers were observed on the surface of the GaAs substrate under polarized light, even though the crystal had shown a decrease in weight. It was obvious that both etching and deposition were working simultaneously in this system. Epitaxial deposits from 2 to 150 microns in thickness have been formed on GaAs substrates. X-ray analysis of the deposits have shown them to be single crystal

TABLE IX Results of Epitaxial Growth Experiments (GaP)

Run	Source Wt. Loss	Temperature °C Source	Seed	HCL Flow cc/Min.	H_2 Flow cc/Min.	Time Min.	Substrate	Seed Weight Gain(grams)
25.	GaP 0.4844	870	735	3	25	90	GaAs (A)	0.0000 0.0001 0.0001
26.	GaP 0.3535	870	763	3	25	60	GaAs (A)	-0.0001
27.	GaP 0.313	870	700	3	25	60	GaAs (A)	---
28.	GaP 0.6560	870	765	3	25	60	GaAs (A)	-0.0028
29.	GaP 0.7170	885	735	4	40	60	GaAs (A)	--
30.	GaP 0.4893	870	765	3	25	60	GaAs (A)	--
31.	Ga loss 0.45	970	737	4	25	80	GaAs (A)	0.0012
32.	Ga- P-	970	735	3	30	55	GaAs (A)	0.0035
33.	Ga- P-	970	735	3	None	60	GaAs (A)	0.0021
34.	Ga-.3127 P-4306	970	735	3	30	45	GaAs (A)	0.0013
35.	Ga-0.2802 P-0.4182	970	770	4.0	30	45	GaAs	0.0012
36.	Ga-0.4701 P-0.4896	970	737	3.0	30	75	GaP	0.0010
37.	Ga-0.3831 P-0 5158	970	737	3.0	30	60	GaP	0.0029

(cont.) TABLE IX Results of Epitaxial Growth Experiments (GaP)

Run	Source Wt. Loss	Temperature Source	°C Seed	HCL Flow cc/Min.	H_2 Flow cc/Min.	Time Min.	Substrate	Seed Weight Gain(grams)
38.	Ga-0.3159 P-0.683	970	830	3.0	30	60	GaP	0.0134
39.	Ga-0.3160 P-0.5048	970	835	3.0	30	60	GaAs	0.0054
40.	Ga-0.5007 P-0.646	970	835	3.0	30	70	GaAs	+0.0008 (Something observed)
41.	Ga-0.369 P-0.585	970	850	3.0	30	60	GaAs	0.0075
42.	Ga-0.276 P-0.954	970	850	3.0	25	60	GaAs	0.0084
43.	Ga-0.408 P-0.609	970	850	3.0	25	90	GaAs	0.0010 (slight gain)
44.	Ga-0.205 P-0.297	950	855	3.	25	70	GaAs (A)	slight loss - (GaP observed on surface) etching + deposition

(cont.) TABLE IX Results of Epitaxial Growth Experiment (GaP)

Run	Source Wt. Loss	Temperature °C Source	Seed	HCL Flow cc/Min.	H_2 Flow cc/Min.	Time Min.	Substrate	Seed Weight Gain(grams)
66.	GaP 0.937	945	850	3.0	20	120	GaAs	0.1092
67.	GaP 0.9662	945	765	3.0	20	125	GaAs	0.0062
68.	GaP 0.9112	945	830	3.0	20	120	Ge	loss
69.	GaP 0.9846	945	795	3.0	20	120	Ge	0.0094
70.	GaP 1.3927	945	795	3.0	20	240	Ge	0.0324
*80	GaP 0.7710	945	795	3.0	20	120	Ge	0.0070
**81	GaP 0.4473	945	795	3.0	20	180	Ge	0.0021

* Zinc at 400°C used as a dopant in the system.

** Antimony at 400°C used as a dopant in the system.

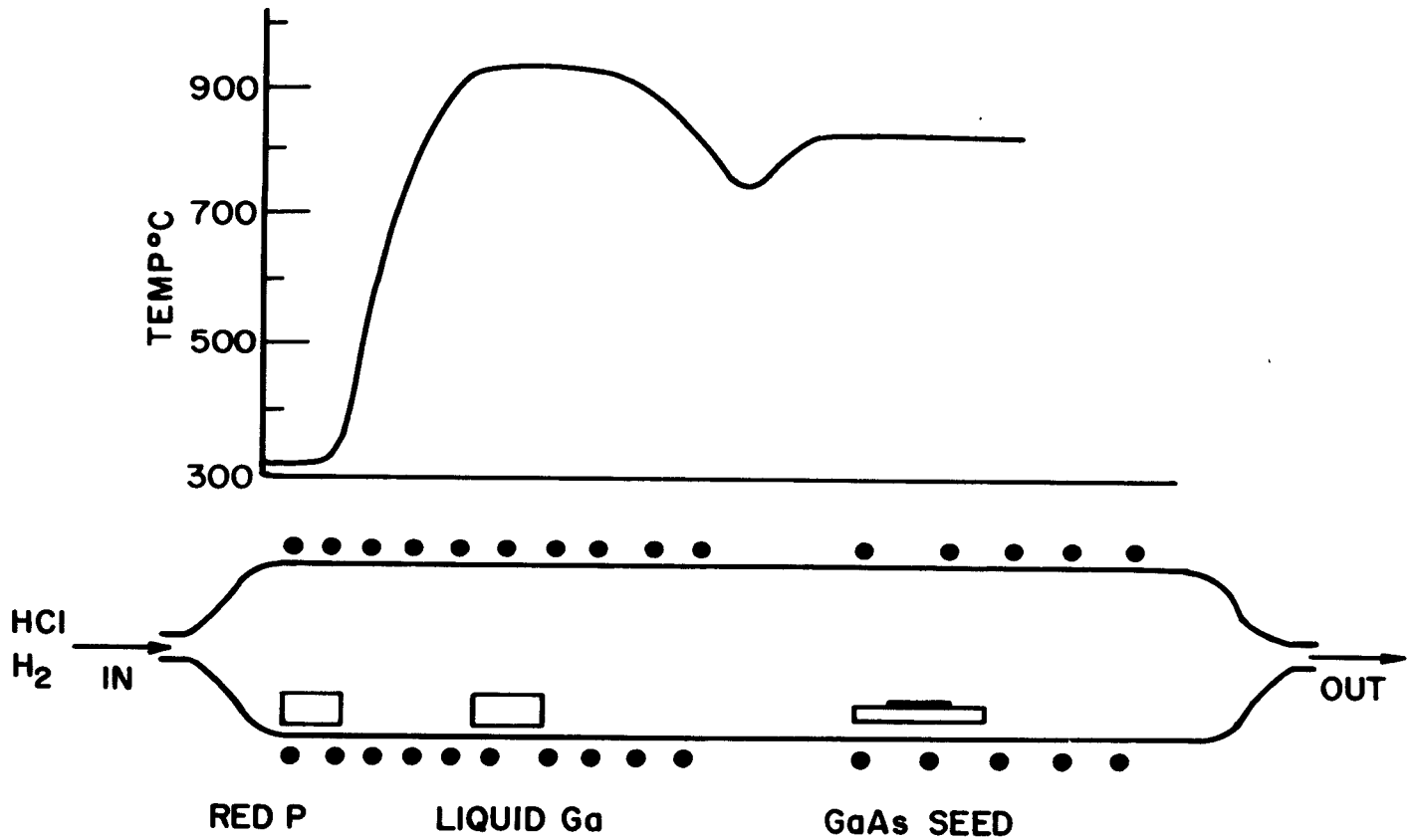


FIG. 45 GaP EPITAXIAL DEPOSITION SET-UP

and to possess the same orientation as the substrate. The photomicrograph shown in Fig. 46 shows a polycrystalline deposit of GaP on a polycrystalline sample of GaP. In the upper section a polycrystalline layer has completely covered the lower substrate material. In the lower section, the GaP layer has remained transparent to light. The substrate's polycrystalline structure is still apparent. Fig. 47 shows some GaP growth facets on a GaP substrate. In all cases the GaP deposits appeared grey in the visible; however, when placed under polarized light the red appearance of GaP became evident. Fig. 48 is a photomicrograph of GaP as it appeared under polarized light. The deposit in this case is extremely thick, approximately 150 microns, and polycrystalline.

It is apparent that the temperature of the substrate material is much more critical in the formation of epitaxial GaP layers than it was in the case of GaAs. The critical temperature for gallium phosphide single crystal epitaxial deposition appears to be $800^{\circ}C \pm 5^{\circ}C$. Reproducible rates of GaP epitaxial growth have been obtained using this substrate temperature and either previously synthesized GaP or Ga and P as source materials. The epitaxial films were in general of a much more facetted nature than those of GaAs. A typical surface of a GaP film deposited on GaAs is shown in Fig. 49.

(ii) Electrical Evaluation of Epitaxial Deposits

Varactor diodes of the same type as those prepared using GaAs epitaxial material, have been prepared from several crystals of GaP. It should be kept in mind that in all cases the substrate material was GaAs. Data obtained from the GaP diodes are given in Table X. One of the first points which becomes evident is that extremely high Q varactor diodes can be made with epitaxial GaP material. This is in direct conflict with the theory that mobility is the limiting factor in the efficiency of a high frequency microwave device, such as a varactor diode. Another interesting point is the effect of the epitaxial layer thickness upon the ϕ obtained from these diodes. The value of ϕ obtained for GaAs point contact diodes is between 1 and 1.3. The value of ϕ obtained for GaP epitaxial material varies from 1.5 to 1.8. If one looks at ϕ as some sort of measure

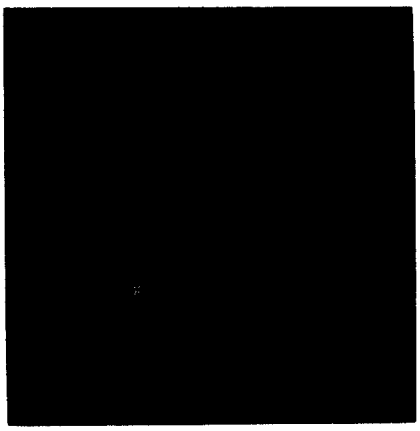


FIG. 46 Deposition of Polycrystalline GaP onto a Polycrystalline Seed of GaP (unetched) 9X

FIG. 47 Growth Facets on GaP (unetched) 50X

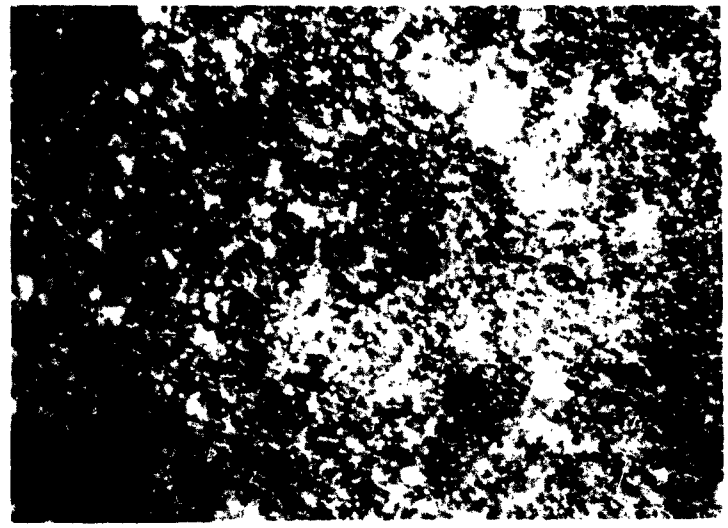


FIG. 48 Polycrystalline Deposit of GaP on GaAs Under Polarized Light, 100X

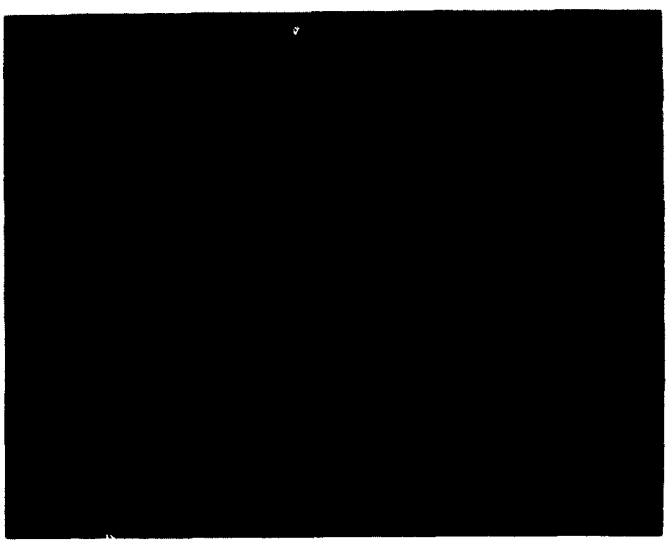


FIG. 49 Facetted Surface of GaP Deposit on GaAs (unetched) 300X

FIG. 50 Open Triangular Defect on GaAs Film Deposited on Ge (unetched) 300X

TABLE X

Electrical Properties of GaP (on GaAs) Varactor Diodes

Sample		V_b	V_f	C_o Pfd	f_c at -2 V(KMC)	ϕ	n_f 2 log 1/aV
Run #40 GaP-1- 6μ thick	(1)	3.0	1.04	.734	187	1.53	1.7
"	(2)	2.8	.93	.518	132	1.6	3.3
"	(3)	3.5	1.14	.712	50		
Monsanto GaAs substrate used for Run #40	(1)	2.6	1.13	.610	90	1.0	
	(2)	1.6	1.07	.450	48	1.0	2.54
	(3)	1.5	.95	.492	0	1.0	
Run #41		7.5	2.75	.522	0	1.65	3.4
Run #42		3.75	2.3	.714	0	1.85	3.3

of the energy gap, values obtained for GaP appeared to correspond well with those obtained for epitaxial GaAs. It is also evident that as the thickness of the GaP layer increases, the ϕ of the device also increases. With the devices that were prepared from thin layer GaP material, it may be that the active region encompassed both GaAs and GaP. The formation of a graded region between GaP and GaAs has already been reported by Holonyak[12]. Diodes prepared from material of runs #41 and #42 produced microwave shorts (no VSWR). This is obviously due to the extremely thick layer of GaP which introduced an extremely high R_s. In order to further check the validity of the results obtained from material prepared in run #40, diodes were made from the basic Monsanto GaAs substrate material 0.0007Ω-cm.

As can be seen, the characteristics of these devices were very poor, substantiating the contribution of the GaP to the microwave properties of the device. All the devices prepared with the GaP were square law devices, therefore allowing accurate determination of ϕ.

D. HETEROJUNCTIONS

Junctions between two semiconductors of the same element, but with different impurities, have been studied extensively. These junctions are well understood. Little work, however, has been done on junctions between two different semiconductors. With the advent, however, of sophisticated techniques of epitaxial growth from the vapor and from solution, it has now become possible to prepare junctions of two different semiconductors. These junctions will be referred to as heterojunctions in the following analysis.

1. Fabrication

(a) GaAs (N) on Ge (P^+)

Using the same experimental set-up and parameters as were discussed for the deposition of GaAs on GaAs, single crystal epitaxial films of GaAs have been grown onto Ge substrates. The only variation was that of the surface preparation of the substrate Ge. The Ge surface was prepared by a chemical polishing technique, using H_2O_2:NaOH in conjunction with an alumina (1μ) soaked cotton pad. GaAs films prepared on Ge substrates were extremely perfect. The defect structures observed were

considerably different from those observed when GaAs is deposited on GaAs. The open triangular defect shown in Fig. 50 is usually found during epitaxial growth of germanium or silicon. Fig. 51 shows the perfect nature of the junction between the GaAs and Ge.

(b) GaAs (P) on GaP (N)

Heterojunctions of GaP-GaAs have been produced by the solution growth technique (TSM) previously described and by the epitaxial growth from the vapor phase of GaP on GaAs. The surface of the GaP epitaxially grown deposit on GaAs is shown in Fig. 49. These deposits for the most part were extremely facetted, the facet structures being mainly of the pyramidal type. The resistivity of the GaP deposited was extremely high, approximately 10^4 to 10^6 Ω-cm; therefore, devices were not prepared from this material. The GaP-GaAs heterojunctions examined were all prepared by the solution growth technique. In this case, a liquid gallium zone was used as the solvent. GaP was the seed crystal and GaAs was the dissolving source crystal. A temperature gradient of 170°C was placed across the sample, the lower solid-liquid interface being at 700°C. The regrown GaAs was found to be single crystal and to possess the orientation of the GaP seed crystal. The regrown GaAs (Ge-doped) was high conductivity P-type.

(c) GaP (N) on Ge (P)

Single crystal oriented GaP films have been deposited on Ge by the HCl vapor transport technique. In this case, the substrate temperature was extremely critical. Deviations of $\pm$ 5°C from the desired temperature 795°C produced microcrystalline yellow deposits of GaP. The surface of the GaP film deposited on Ge is shown in Fig. 52. As can be seen, the elongated pyramidal facets covered the entire surface. A polished cross-section of the GaP-Ge structure (Fig. 53) showed the junction to be highly perfect. On etching, however, (Fig. 54) a diffusion region could be observed. Such a composite structure between Ge and GaP has not been previously reported in the literature. The erratic results obtained with these junctions may be a consequence of this rather thick (2μ) transition region.

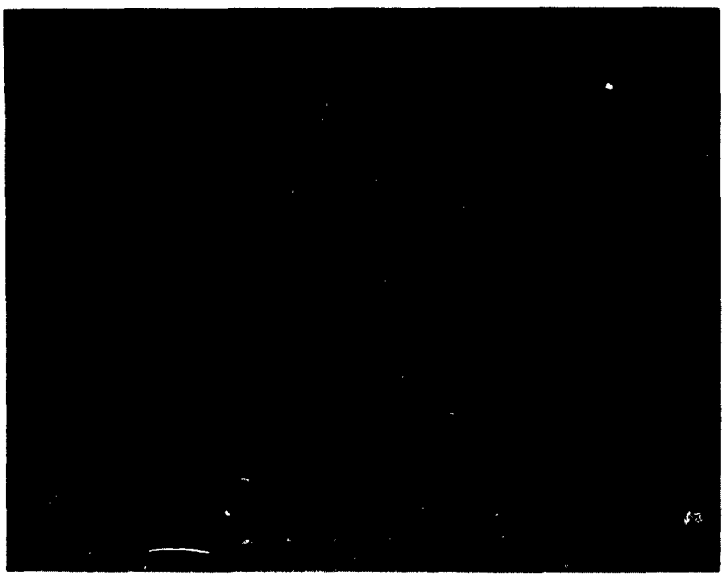


FIG. 51 Junction Between GaAs and Ge (250X)

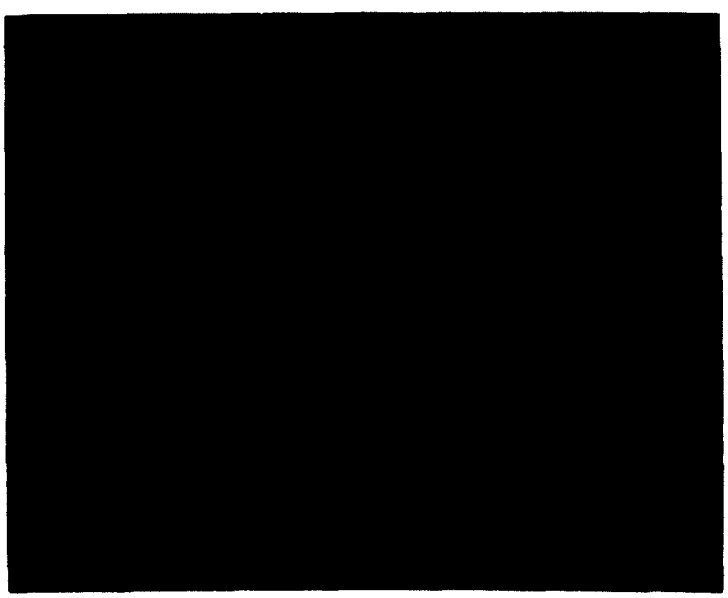


FIG. 52 Surface of GaP Film Deposited on Ge (100X)

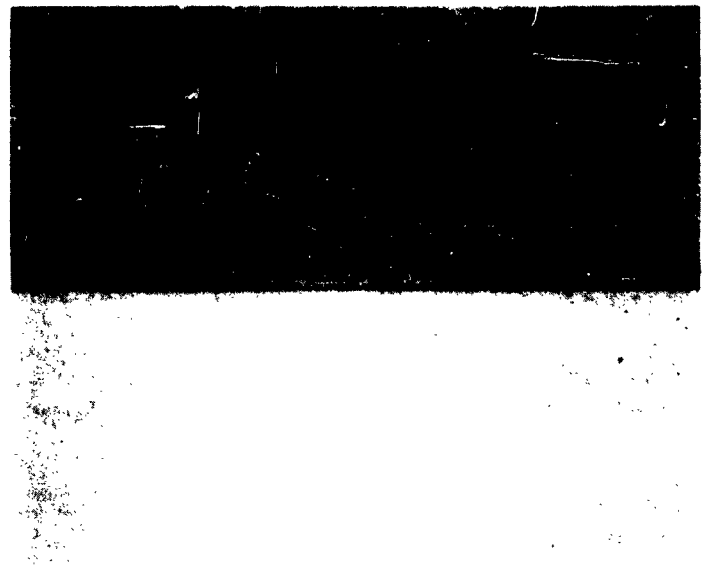


FIG. 53 Polished Cross-Section of GaP-Ge Junction (20° angle lap) 1000X

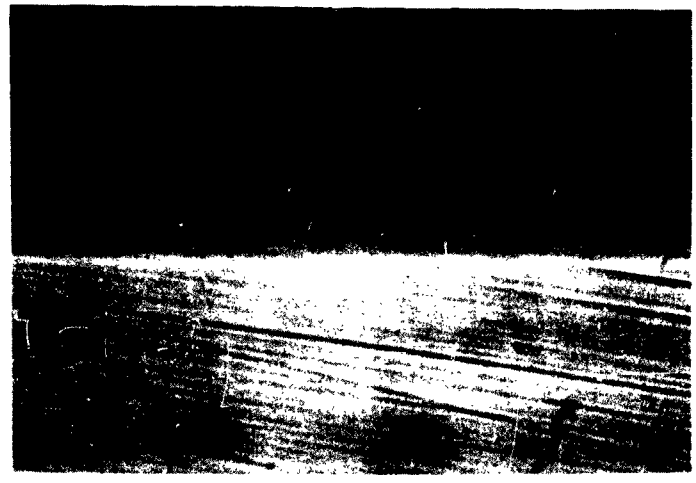


FIG. 54 Etched Cross-Section of GaP-Ge Junction Showing Transition Region (20° angle lap) 1000X

2. Electrical Evaluation

The abrupt junction character of all the hererojunctions studied has been confirmed by capacitance as a function of reverse bias measurements. All the diodes showed square law behavior, with ϕ values (built-in potential) intermediate between that of the two constituent semiconductors. The values of built-in potential of all the junctions studied are given in Table XI.

(a) GaAs (N) on Ge (P)

This heterojunction consisted of 0.001 Ω-cm N-type GaAs and 0.002 Ω-cm Ge. The ohmic contacts used were Au : Sn for the GaAs (N) and In : Ag for the Ge (P). A ceramic package was used to encapsulate these diodes. The V-I characteristic of this heterojunction was studied as a function of temperature. In Fig. 55 the oscilloscope traces of the forward characteristics at 23, 80, and 158°C are shown. As can be seen, the forward currents for a diode of this area (0.2 cm^2) are definitely higher than those which would be expected for GaAs. The reverse characteristics are shown in Fig. 56. Even though the reverse characteristic is not extremely sharp, it is obvious that the leakage current is determined by the weak link of the junction, Ge in this case. As can be seen, at 100°C the leakage becomes extremely excessive and past 120°C, where the germanium becomes conductive, the reverse characteristic is almost completely lost. This can be explained by the thermal generation of an electron-hole pair in the Ge. An illustration of this is shown on the energy band diagram of this junction in Fig. 57.

(b) GaP (N) on Ge (P)

All attempts to get consistant electrical results from GaP - Ge heterojunctions have met with failure. Much of this problem is ascribed to the transition region which was observed in this structure and which was explained in the previous section. A typical I-V characteristic for this heterojunction is shown in Figs. 58 A&B. This type of a plot can be explained by a heterojunction which includes an extremely high resistivity transition region (insulating between the two semiconductors). Various attempts to study the resistivity and structure of this insulating layer have been unsuccessful.

TABLE XI

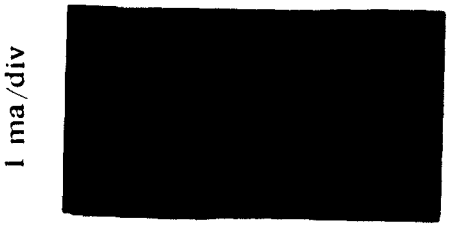
Value of ϕ for Various Junctions

$$C_V = \frac{C_o}{(1 - V/\phi)^{1/2}}$$

Junction	ϕ
Ge (P^{++}) on Ge (N)	0.60
GaAs (P^{++}) on Ge (N)	0.78
GaAs (P^{++}) on GaAs (N)	1.0 - 1.3
GaAs (P^{++}) on GaP (N)	1.8
GaP (P^{++}) on GaP (N)	1.9 - 2.0

I(ma)	Volts
1	.80
2	.88
3	.90
4	.92
5	.94
6	.96

23°C



1 ma/div

1/2 volt/div

1	.62
2	.72
3	.75

80°C

1 ma/div

1/2 volts/div

1	.40
2	.48
3	.53
4	.57
5	.60

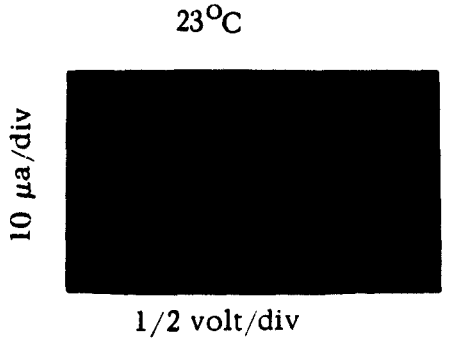
160°C

1 ma/div

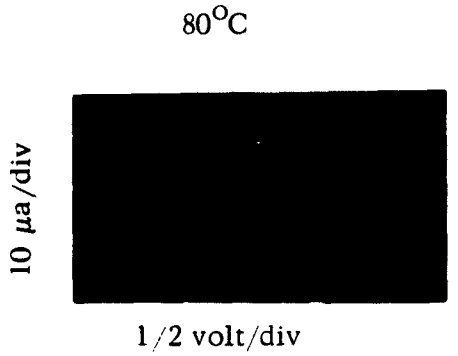
1/2 volts/div

FIG. 55 Forward Characteristics of GaAs-Ge Diode as a Function of Temperature

I(μa)	Volts
10	1.80
20	1.95
30	2.06
40	2.12
50	2.30
100	2.42
150	2.55



10	1.50
20	1.70
30	1.78



10	.40
20	.90
30	1.2
40	1.4
50	1.54
100	1.85
150	2.02
200	2.10
250	2.15

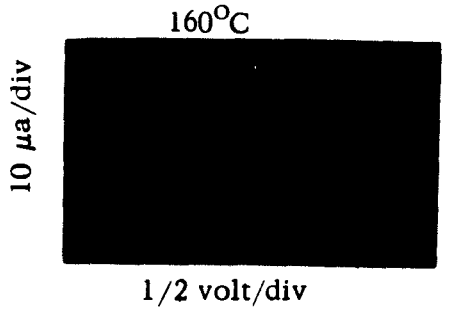
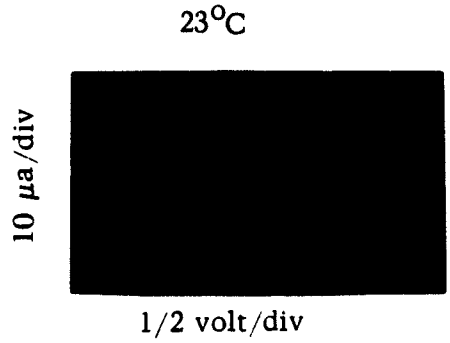
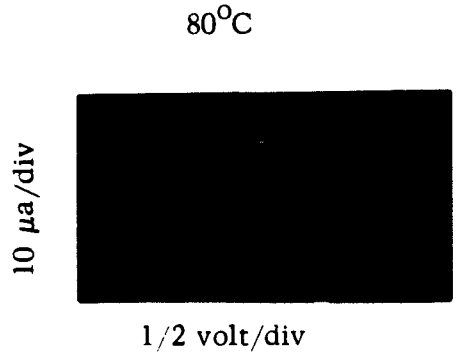


FIG. 56 Reverse Characteristics of GaAs-Ge Diode as a Function of Temperature

I(μa)	Volts
10	1.80
20	1.95
30	2.06
40	2.12
50	2.30
100	2.42
150	2.55



10	1.50
20	1.70
30	1.78



10	.40
20	.90
30	1.2
40	1.4
50	1.54
100	1.85
150	2.02
200	2.10
250	2.15

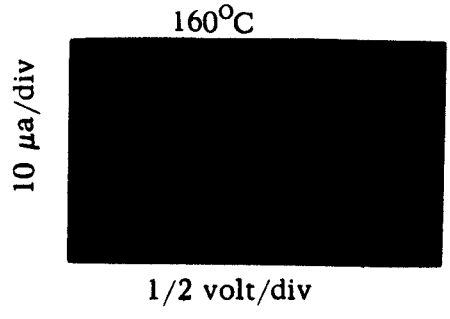


FIG. 56 Reverse Characteristics of GaAs-Ge Diode as a Function of Temperature

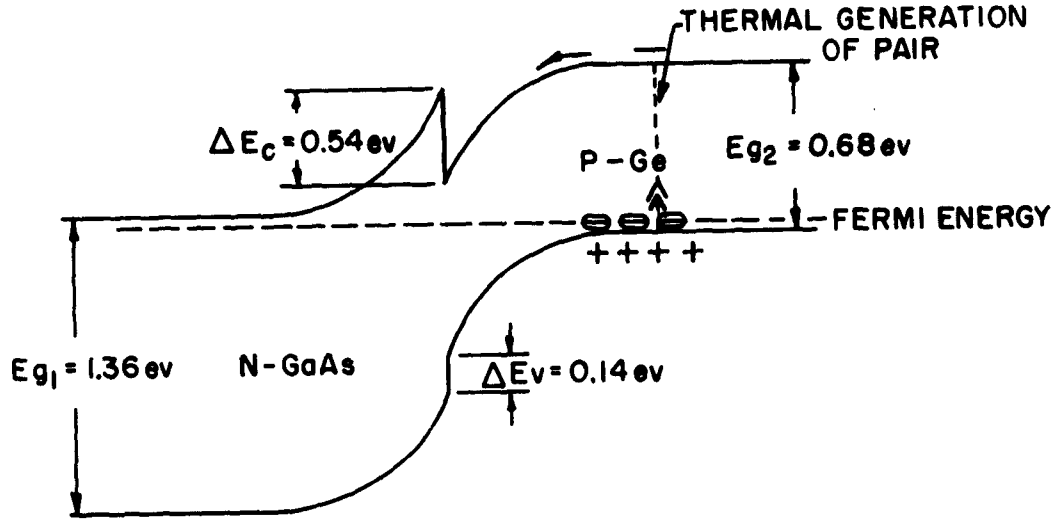


FIG. 57 Energy Band Diagram of GaAs-Ge Heterojunction

FIG. 58A Forward I-V Characteristic of GaP Heterojunction as a Function of Temperature

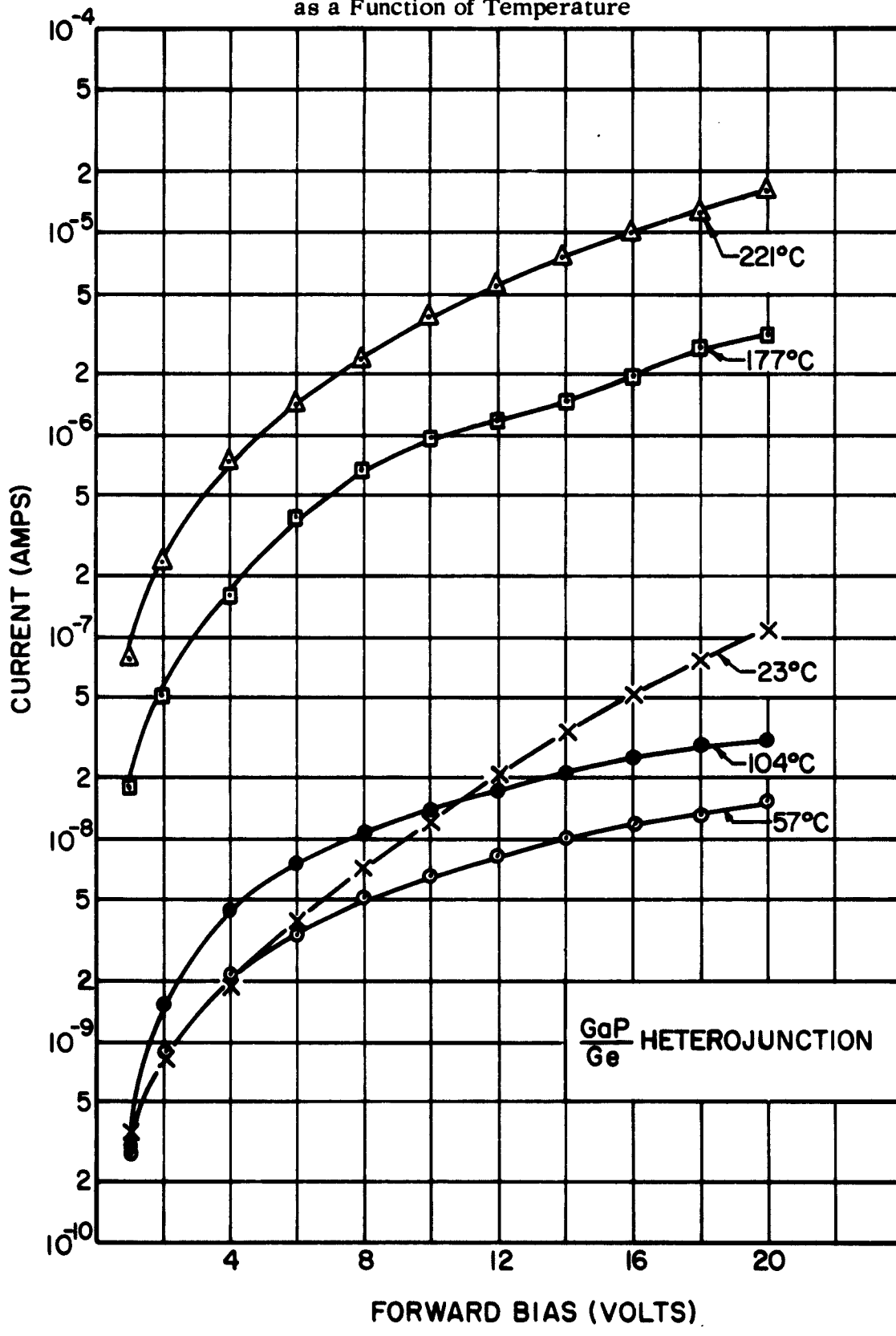
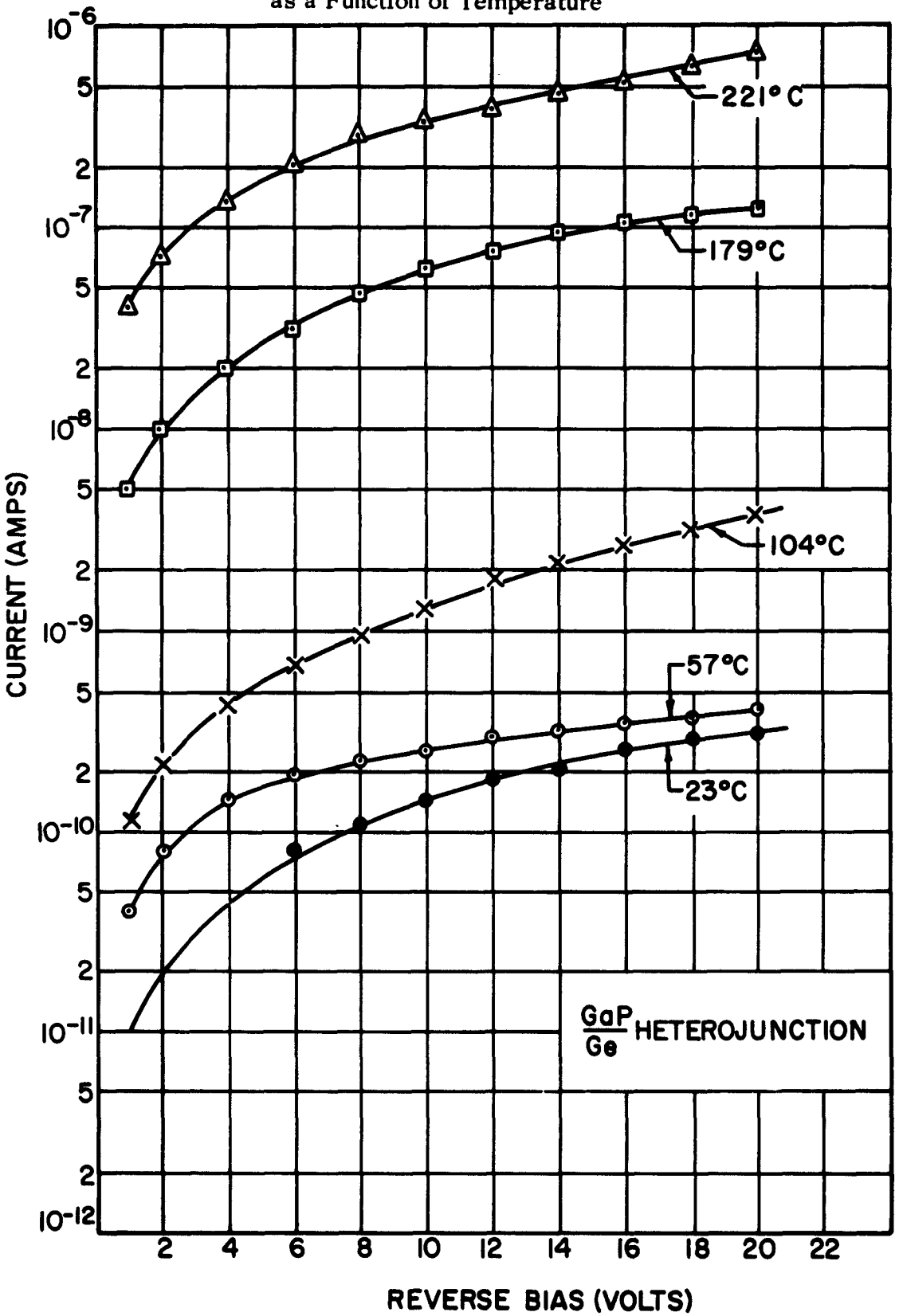


FIG. 58B Reverse I-V Characteristic of GaP-Ge Heterojunction as a Function of Temperature



(c) GaP (N) on GaAs (P)

A particularly interesting P-N heterojunction is formed when P-type GaAs (0.0006 Ω- cm) is deposited on N-type GaP (0.01 Ω-cm). If a semi-logarithmic plot is made of current vs. voltage (Fig. 59) a curve with several kinks is observed. Fig. 60 shows the energy band structure of such a heterojunction. The energy gap of GaAs is about 1.4 ev and that of GaP is 2.0 ev, so that $\Delta E_c + \Delta E_v = 0.7$ ev. The curve may be divided into four regions. In each region the current can be roughly approximated by the exptression:

$$I = I_o \exp \left\{ ev/\eta kT \right\} \qquad (29)$$

where η is some number characterizing the slope. In region I the current is carried by electrons flowing across the junction. As the voltage is increased, because of the discontinuity of the conduction band, the current does not increase as rapidly (Region II). With a further increase in voltage, conduction via holes becomes important (Region III). Finally the ohmic resistance of the material becomes important in limiting the current. The diode conducts about 10 μA with 7 volts reverse bias.

Measurements were made at several temperatures between 104°C and -195°C, and in all cases the same general form for the current-voltage curve was observed. Similar behavior has been reported by R. L. Anderson[13] for a GaAs-Ge heterojunction, but without as clearly a defined plateau region.

Capacity measurements were made at room temperature as a function of bias. The data can be fit quite well by square law plot:

$$1/C^2 = 1/C_o^2 \, (1-V/\phi) \qquad (30)$$

where $\phi \approx 1.8$ volts for reverse bias and $\phi \approx 1.5$ when biased in the forward direction.

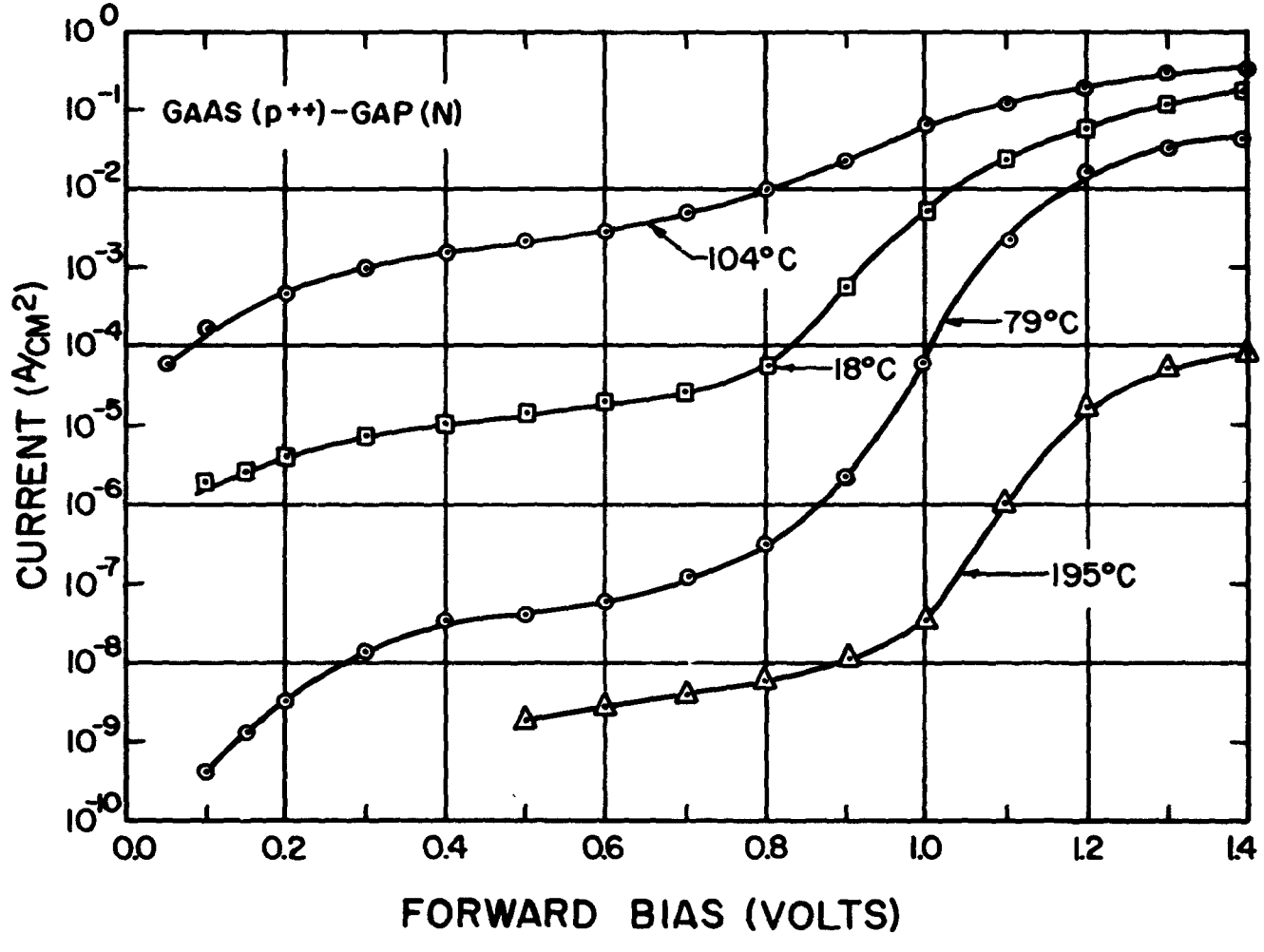


FIG. 59 Forward I-V Characteristic of GaP-GaAs Heterojunction as a Function of Temperature

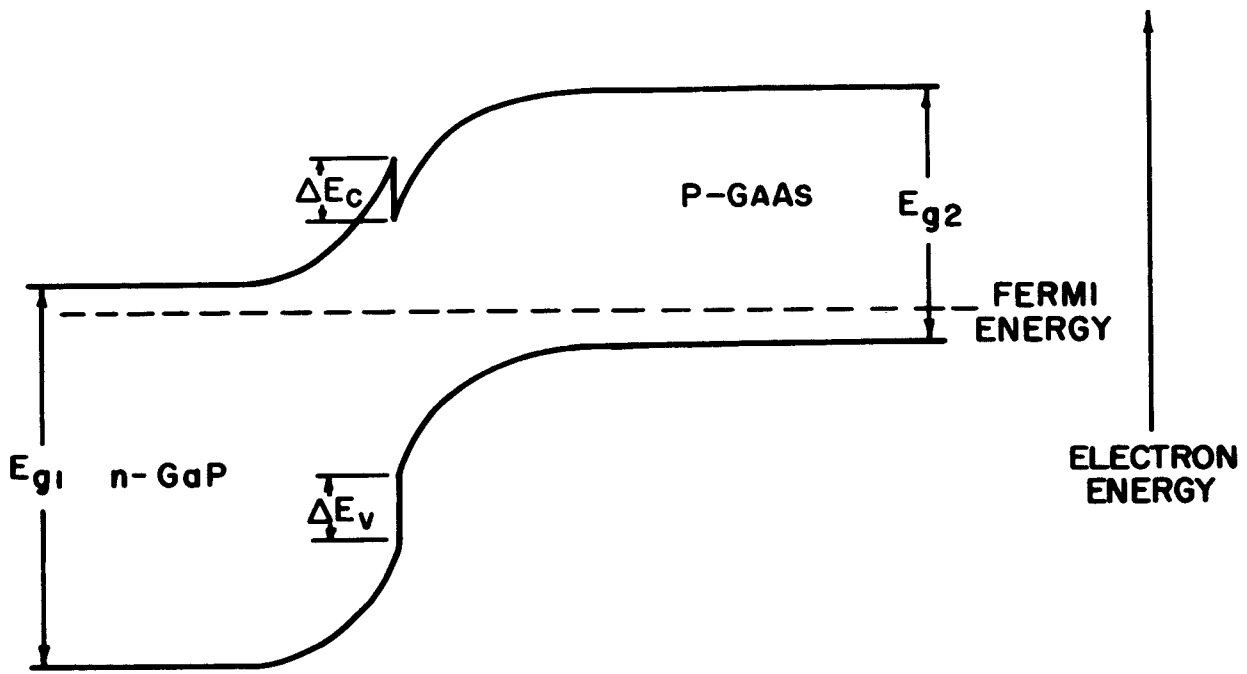


FIG. 60 Energy Band Diagram of GaAs-GaP Heterojunction

TABLE XII

Value of η in Expression $I = I_o \exp(ev/\eta kT)$

For Different Ranges of Voltage in A

GaAs-GaP Heterojunction

Temp	η ($I = I_o \exp(ev/\eta kT)$)		
^oC	0 - 0.3V	0.3 - 0.8V	0.8 - 1.2V
104	1.7	15	1.9
18	1.9	15	1.3
-79	1.8	18	1.4
-195	-	44	3.8

IV. SUMMARY

1. Low pump power-square law varactor diodes have been fabricated with cut-off frequencies up to 750 KMC at breakdown.

2. Large area P^{++} on N GaAs junctions have been prepared by alloying techniques. They exhibit square-law behavior up to breakdown.

3. The breakdown voltage of the P^{++} on N GaAs diodes follows the relationship:

$$V_b = 10 \quad N^{-0.58}$$

where N = carrier concentration of the N-type GaAs.

4. The epitaxial growth of GaAs and GaP on GaP, GaAs and Ge substrates has been accomplished by vapor phase and solution techniques.

5. Point contact varactor diodes utilizing GaP (deposited on low resistivity GaAs) as the active semiconductor have cut-off frequencies of 187 KMC at -2V.

6. The electrical properties of GaAs-Ge and GaP-GaAs heterojunctions have been determined. Various kinks are observed in the I-V characteristic of the GaP-GaAs heterojunction. The kinks can be explained by discontinuities in the energy band structure. The reverse leakage current of the GaAs-Ge junction at various temperatures is determined by the Ge portion of the junctions.

V. PAPERS AND PUBLICATIONS

1. The Voltage Breakdown of GaAs Abrupt Junctions
   Martin Weinstein and A. I. Mlavsky, Appl. Phys. Letters, 2, No. 5, pp 97-99 (1963)

2. The Capacitance of GaAs Abrupt Junctions
   Martin Weinstein and A. I. Mlavsky, in course of preparation

3. Preparation and Properties of Epitaxial GaAs-GaP, GaAs-Ge, and GaP-Ge Heterojunctions
   Martin Weinstein, A. A. Menna and A. I. Mlavsky, presented at the Meeting of the Electrochemical Society, Pittsburgh, 1963

4. Grown P-N Junctions in SiC, GaAs and GaP
   L. B. Griffiths, A. I. Mlavsky and Martin Weinstein, presented at the Meeting of the Electrochemical Society, Pittsburgh, 1963

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13 R. L. Anderson, J. Solid State Electronics, 5, 341 (1962)

VII. TECHNICAL CONTRIBUTORS

Name	Hours
Airy, J.	171
Bell, R.	696
Boutelier, R.	150
Cohen, S.	220
Demeo, F.	144
Ford, J.	4
Fuller, T.	2
LaBelle, H.	1744-1/2
Menna, A. A.	838
Mlavsky, A. I.	498
Roode, R.	1196
Shaw, B. A.	72
Tsouvalas, E.	300
Weinstein, M.	1215
Wright, M. A.	144
total	7394-1/2